MT6205B GSM Baseband Processor Data Sheet

Revision 1.03

October 15, 2003

Revision History

Revision	Date	Author	Comments
1.00	Mar. 27, 2003	Cliff	First release.
1.01	Mar. 28, 2003	Cliff	Add CSD
1.02	Apr.23, 2003	Cliff	Update Aux ADC, APC, AFC and UART
1.03	Oct.15, 2003	Cliff	Update RTC and PDN

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1. System Overview

The MT6205B is a highly integrated baseband processor optimized specially for multi-media enabled GSM terminal. Combining the 32-bit ARM7TDMI^{TM} RISC processor core, proprietary low-power digital signal processor, user interface, radio control, audio codec, baseband codec, and other GSM specific analog and digital hardware, the MT6205B completes the best single-chip solution for GSM phone with multi-media function. The typical application can be shown as **Figure** 1.

External Memory Interface

With the External Memory Interface, the MT6205B can supports varieties of SRAM and Flash in the market and multi-media devices with parallel interface, such as color LCD panel, MIDI synthesizer and Digital Still Camera etc. Regarding the consideration of power consumption and low noise, this interface is designed for flexible I/O voltage and allows for lowering supply voltage down to 1.8V. In addition, the driving strength is configurable that makes the signal integrity problem easy. Retention technology is also specifically used on data bus to prevent the bus from being floating during turn over.

User Interface

For user interactions, the MT6205B brings together all necessary peripheral blocks for a value-added GSM phone. It comprises the Keypad Scanner, SIM Controller, dual channels UART, Alerter, Real Time Clock, PWM, Serial LCD Controller and General Purpose Programmable I/Os. In addition to adequate pull up or pull down included in the PAD cells, the MT6205B minimizes external components and reduces cost and size required for PCB. Besides, DMA (Direct Memory Access) and hardware flow control for SIM Controller and UART are implemented, that greatly enhances the performance and helps to reserve processing power.

Audio Interface

Two microphone inputs with one low noise amplifier as well as two audio output with two power amplifiers are contained. Incorporating with on-chip mixed-signal Audio Front-End, this complete architecture allows for easy audio interfacing with direct connection to the audio transducers. In addition, the MT6205B gives also the flexibility for developer to modify the frequency response of digital filter in compensating the effects from acoustic devices.

Radio Interface

Providing a well-organized interface with the radio part, the MT6205B integrates programmable AFC (Automatic Frequency Control), APC (Automatic Power Ramping Control), the Parallel (BPI) and Serial (BSI) RF control circuitry and on-chip mixed-signal Baseband Front-End. It carries out also gain and offset calibration mechanisms and filters with programmable coefficients to fulfill the MODEM function. The approach is also towards combining a high resolution 13-bit D/A Converter with VCXO or crystal to reduce the overall system cost. Besides, to remove the necessary of external current-driving component, the driving strength of some BPI outputs is designed to be configurable. Accompanying with RF Tools, the MT6205B based system provides developer with flexibility for efficient customization as well as comprehensive compatibility control on RF modules.

Debug Function

The JTAG interface enables in-circuit debugging of software program with the embedded ARM7TDMI core. With this standardized debugger interface, the MT6205B provides developers with a wide set of options for choosing ARM development kits from supports of thirty parties.

Power Management

The MT6205B offers various low-power features helping reduce system power consumption including Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals and Processor Sleep Mode. Fabricated in low-leakage CMOS process, together with the low-power features, the overall system can achieve ultra low power consumption.

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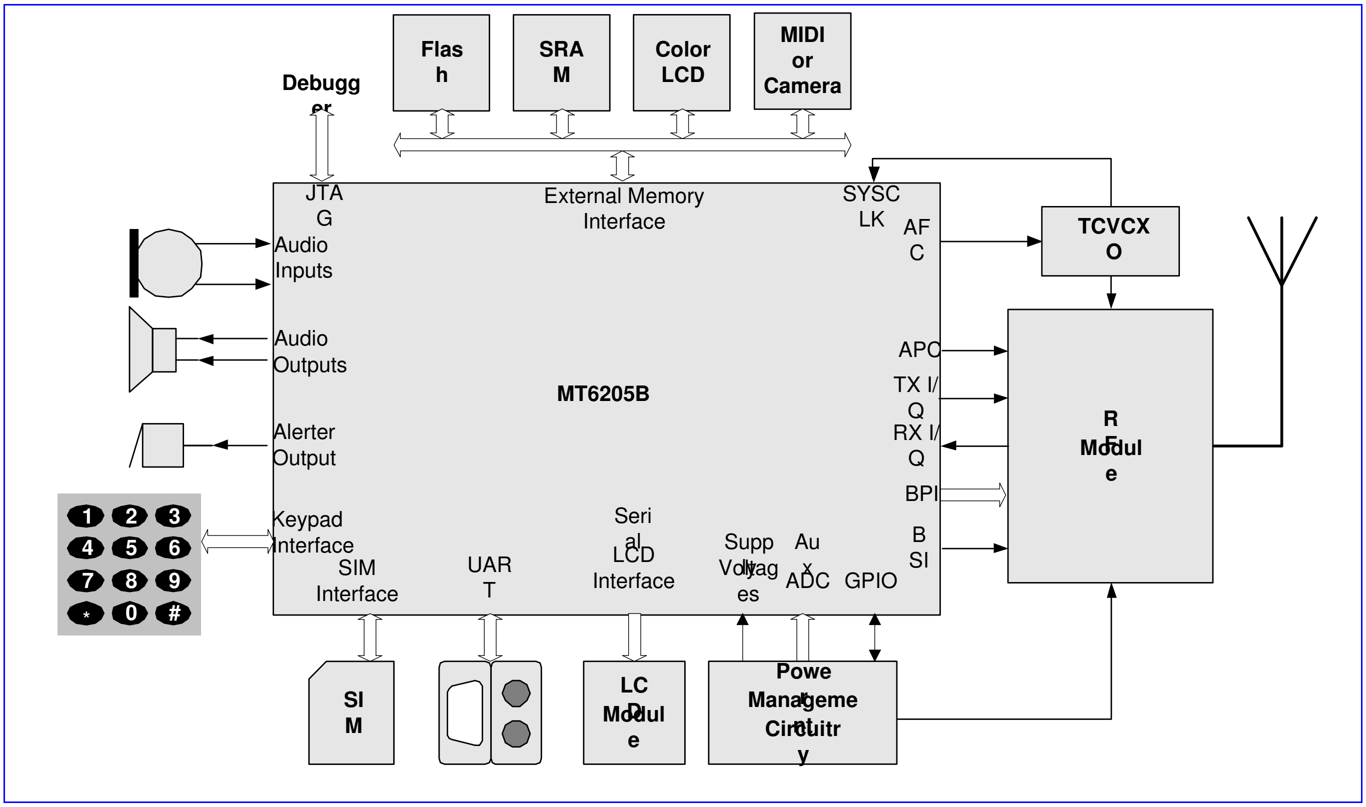

Figure 1 Typical application of MT6205B

1.1 Features

- **General**
  - Dual-core architecture
  - Integrated voice-band and base-band analog front ends
  - 0.18µm low-leakage CMOS process, 1.8V core voltage
  - TFBGA 12mm×12mm 0.8mm pitch 181 package
- **MCU System and External Memory Interface**
  - ARM7TDMI 32-bit low-power RISC processor supporting THUMB instruction set
  - AMBA internal bus
  - Operating frequency: 13/26 MHz
  - 2 Generic DMA channels for UART and SIM Controller
  - Dedicate DMA channel for color LCD panel
  - 32K Bytes zero-wait-state on-chip SRAM
  - On-chip boot ROM for Factory Flash Programming
  - Watchdog timer for system crash recovery
  - General-purpose timers
  - Division and Circuit-Switch-Data coprocessors
  - Supports external 8-bit or 16-bit Flash and SRAM with size up to 16M Bytes each
  - Supports Flash with Page Mode
  - Supports up to 4 external devices with memory interface
  - Supports color LCD panel with acceleration function for frame refreshing
  - Flexible I/O voltage of 1.8V ~ 3V for memory interface
  - Configurable driving strength for memory interface
- **Voice and Baseband Codec**
  - GSM Phase 2 speech coding support including enhanced full rate, full rate and half rate (EFR/FR/HR)
  - Provide data service in standard circuit-switched mode
  - Melody generation with up to 16 tones
  - Wavetable synthesis with up to 16 notes
  - Dial tone generation
  - Voice Memo

- PCM Playback
- Digital sidetone generator with programmable gain
- Two 30-tap programmable acoustic compensation filters
- GSM channel coding, equalization and A5/1 and A5/2 ciphering
- GSM Modem with programmable coefficients

■ **User Interfaces**

- 5-row × 5-column keypad controller with hardware scanner
- 3V SIM Card Controller with hardware flow control
- 2 Channels of UART with hardware flow control and auto baud detection, speed up to 115200 bps
- Real Time Clock (RTC) operating with a separate power supply
- 2 Channels Serial LCD Interface with 7 bytes TX FIFO
- Industrial standard Parallel LCD Interface
- General Purpose I/Os (GPIOs)
- 2 Sets of Pulse Width Modulation (PWM) Output
- Alerter Output with Enhanced PWM or PDM
- Four external interrupt lines

■ **Audio Interface and Audio Front End**

- Two microphone inputs sharing one low noise amplifier with programmable gain
- Two Audio power amplifiers with programmable gain
- 2nd order Sigma-Delta A/D Converter for uplink path
- D/A Converter for downlink path
- Support half-duplex hands-free operation
- Complying with GSM 03.50

■ **Radio Interface and Baseband Front End**

- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A Converter for uplink baseband I and Q signals
- 11-bit A/D Converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
- 10-bit D/A Converter for Automatic Power Control
- 13-bit high resolution D/A Converter for Automatic Frequency Control
- Programmable Radio RX filter with 31 taps

- 2 Channels Baseband Serial Interface (BSI) with 3-wire control
- 8-Pin Baseband Parallel Interface (BPI) with programmable driving strength
- Multi-band support

■ **Power Management**

- Power Down Mode for analog and digital circuits
- Processor Sleep Mode
- Pause Mode of 32KHz clocking at Standby State
- 5-channell Auxiliary 10-bit A/D Converter for charger and battery monitoring

■ **Test and Debug**

- Built-in digital and analog loop back modes for both Audio and Baseband Front-End
- DAI port complying with GSM Rec.11.10
- JTAG port for debugging embedded MCU
- Three NAND-trees for I/O testing

1.2 General Description

Figure 2 details the block diagram of MT6205B. Based on dual-processor architecture, the major processor of MT6205B is ARM7TDMI, which takes the main controls of the chip as well as executes high-level GSM protocol software. With the other one is a digital signal processor corresponding for handling the low-level GSM channel coding / decoding and speech compression / decompression. Except for some mixed-signal circuitries, the remaining logics in MT6205B are coupled to either the microcontroller or the digital signal processor. Specifically, MT6205B consists of the following subsystems:

- Microcontroller Unit (MCU) Subsystem, including an ARM7TDMI RISC processor core and its accompanying memory management and interrupt handling logics.
- Digital Signal Processor (DSP) Subsystem, including a DSP and its accompanying memory, memory controller, and interrupt controller.
- MCU/DSP Interface, where the MCU and the DSP exchange hardware and software information.
- Microcontroller Peripherals, which includes user interface modules and some RF control interface modules.
- DSP Peripherals, which are hardware accelerators for GSM channel codec.
- Audio Front End, the data path of conveying analog speech from and to digital speech.
- Baseband Front End, the data path of conveying digital signal form and to analog signal of RF modules.
- Timing Generator, generating the control signals related to the TDMA frame timing.
- Power, Reset and Clock subsystem, managing the power, reset and clock distribution inside MT6205B.

Details of the individual subsystems and blocks are described in following Chapters.

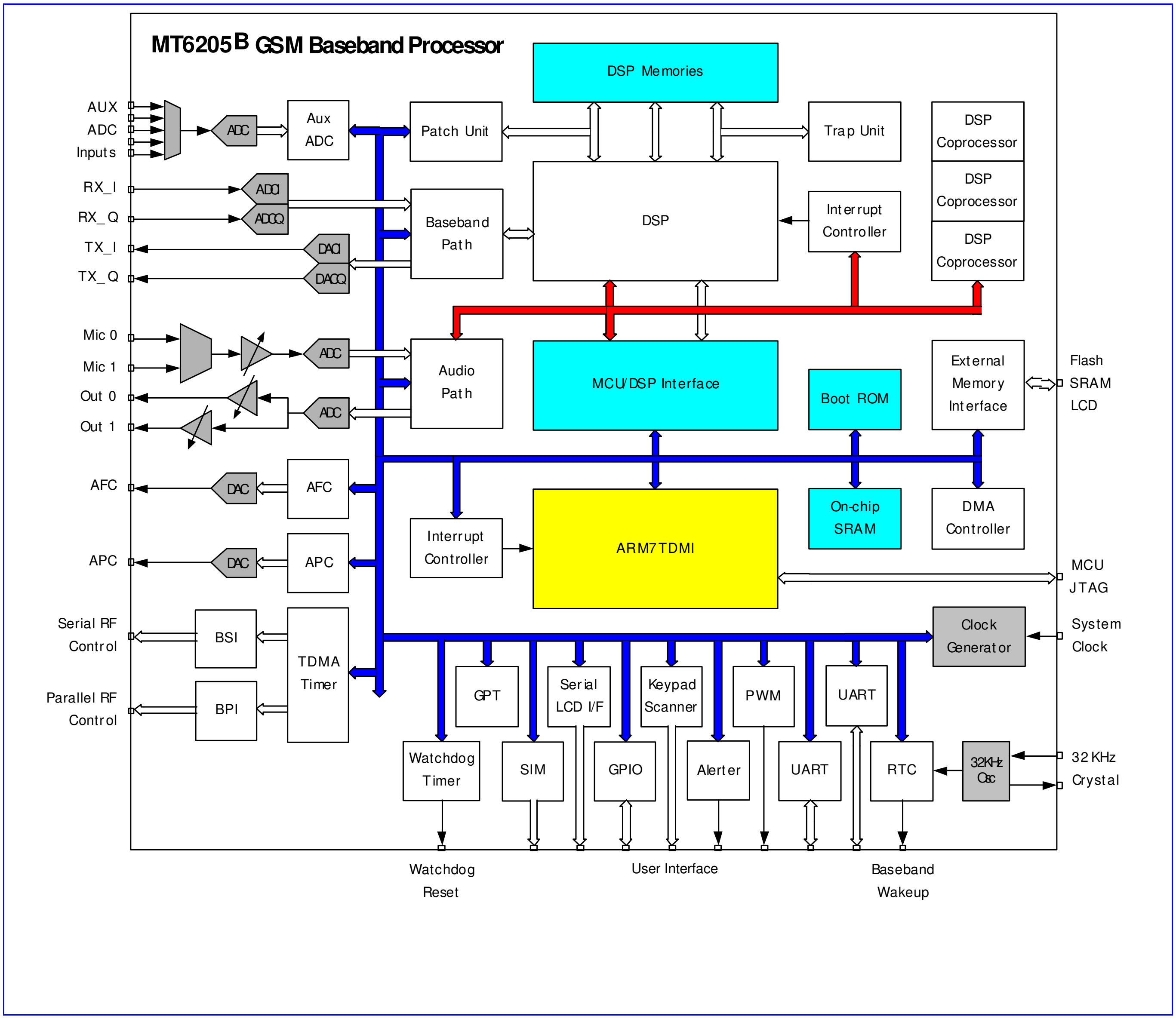

Figure 2 MT6205B block diagram.

2 Product Description

2.1 Pin Outs

One type of package for this product, TFBGA 12mm*12mm 0.8pitch 181, is offered.

Pin outs and the top view are illustrated in **Figure 3** for 181-Ball TFBGA of 12mmx12mm 0.8pitch.

Outline and dimension of package is illustrated in **Figure** 4, while the definition of package is shown in **Table** 1.

MT6205B TFBGA 181 Top-View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	JTDI	XOUT	AVDD_RTC	AFC	AUXADIN3	AVDD_RFE	BUPAIN	BDLAIN	AGND_RFE	AU_VIN0_N	AVDD_AFE	AVSS_BUF	AU_OUT0_P	AU_OUT1_N	A
B	VSS33	BBWAKEUP	XIN	AVDD_PLL	AUXADIN4	APC	BUPAIP	BDLAIP	AVSS_AFE	AU_VIN0_P	AU_MICBIAS_N	AU_OUT0_N	AU_OUT1_P	DAIRST	B
C	JTMS	JTRST#	JTCK	SYSCLK	AUXADIN2	AVDD_GSMRFTX	BUPAQN	BDLAQN	AU_VIN1_P	AGND_AFE	AU_MICBIAS_P	AVDD_BUF	DAIPCMIN	DAIPCMOUT	C
D	VDD33	BPI_BUS0	JTDO	AVSS_PLL	AUX_RFE	AUXADIN0	BUPAQP	BDLAQP	AU_VIN1_N	AU_VREF_P	DAICLK	UREF_CK	VSS33	VDD33	D
E	BPI_BUS5	BPI_BUS3	BPI_BUS4	BPI_BUS2	AFC_BYP	AUXADIN1	AVSS_RFE	AVSS_GSMRFTX	AU_VREF_N	UTXD2	URXD2	URTS1	URTS2	UCTS2	E
F	VDDK	VSSK	BPI_BUS7	BPI_BUS6	BPI_BUS1				TESTMODE	UCTS1	UTXD1	EA23	VSSK	VDDK	F
G	VSS33	PWM1	BSI_CLK	BSI_DATA	BSI_CS0					URXD1	EA22	EA20	EA21	EA19	G
H	LCD_DATA	LCD_CLK	LCD_A0	LCD_CS0#	LCD_CS1#					EA14	EA15	EA17	EA16	EA18	H
J	VDD33	SIMRST	SIMCLK	SIMVCC	GPIO15					EA7	EA11	EA12	EA13	VDD33_EMI	J
K	SIMSEL	SIMDATA	GPIO13	GPIO14	KROW1	EINT2	ED1	ED9	ED13	EWR#	EA8	EA9	VSS33_EMI	EA10	K
L	VSS33	SYSRST#	WATCHDOG#	KROW3	KROW0	ED0	ED2	ED8	ED10	ERD#	ECS1#	EA4	EA5	EA6	L
M	SRCLKENAN	KCOL3	KCOL4	KROW2	EINT1	ECS3#	ED5	ED6	ED12	ED14	ECS0#	EA2	EA1	EA3	M
N	SRCLKENA	KCOL1	KROW4	VSSK	EINT0	ELCDWR#	ED4	ED7	VSS33_EMI	ED15	VSSK	VSS33_EMI	EUB#	VDD33_EMI	N
P	KCOL2	KCOL0	VDD33	VDDK	ALERTER	VSS33	ED3	VDD33_EMI	ED11	VDD33_EMI	VDDK	ECS2#	ELB#	EA0	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3 Top View of MT6205B TFBGA 12mm*12mm 0.8pitch 181 Package

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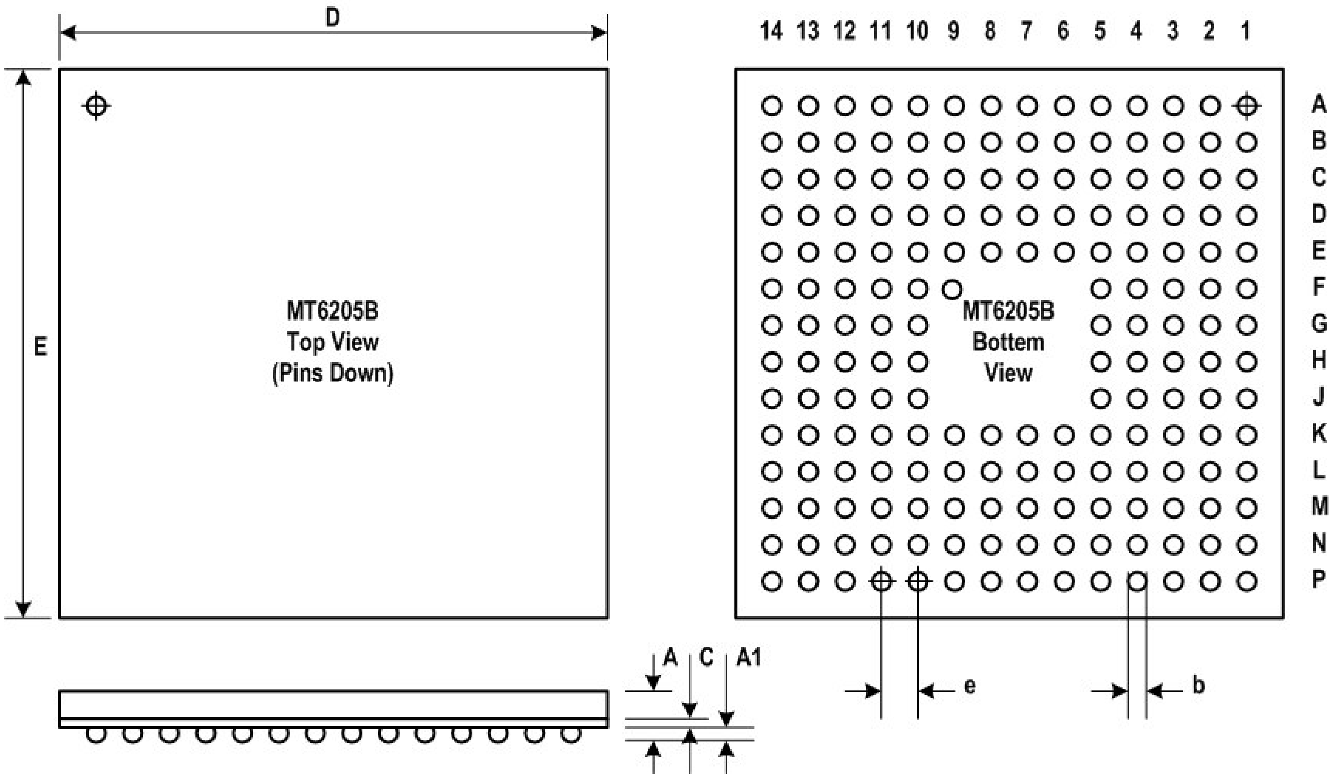

Figure 4 Outlines and Dimension of TFBGA 12mm*12mm 0.8pitch 181

Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	e	b	A (Max.)	A1	C
12	12	181	0.80	0.4	1.4	0.3	0.36

Table 1 Definition of TFBGA 12mm*12mm 0.8pitch 181 (Unit: mm)

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2.2 Pin Description

Ball		Name	Dir	Description	Alt1	Alt2	Pull	Reset
12X12								
JTAG Port								
C2		**JTRST#**	I	JTAG test port reset input			PD	Input
C3		**JTCK**	I	JTAG test port clock input			PU	Input
A1		**JTDI**	I	JTAG test port data input			PU	Input
C1		**JTMS**	I	JTAG test port mode switch			PU	Input
D3		**JTDO**	O	JTAG test port data output				0
RF Parallel Control Unit								
D2		**BPI_BUS0**	O	RF hard-wire control bus 0				0
F5		**BPI_BUS1**	O	RF hard-wire control bus 1				0
E4		**BPI_BUS2**	O	RF hard-wire control bus 2				0
E2		**BPI_BUS3**	O	RF hard-wire control bus 3				0
E3		BPI_BUS4	IO	RF hard-wire control bus 4	**GPIO4**		PD	Input
E1		BPI_BUS5	IO	RF hard-wire control bus 5	**GPIO5**		PD	Input
F4		BPI_BUS6	IO	RF hard-wire control bus 6	**GPIO6**		PD	Input
F3		BPI_BUS7	IO	RF hard-wire control bus 7	**GPIO7**	BSI_CS1	PD	Input
RF Serial Control Unit								
G5		**BSI_CS0**	O	RF 3-wire interface chip select 0				0
G4		**BSI_DATA**	O	RF 3-wire interface data output				0
G3		**BSI_CLK**	O	RF 3-wire interface clock output				0
PWM Interface								
G2		PWM	IO	Pulse width modulated signal for light	**GPIO16**		PD	Input
Serial Display Interface								
H1		LCD_DATA	IO	Serial display interface data output	**GPIO8**		PD	Input
H3		LCD_A0	IO	Serial display interface address output	**GPIO9**		PD	Input
H2		LCD_CLK	IO	Serial display interface clock output	**GPIO10**		PD	Input
H4		LCD_CS0#	IO	Serial display interface chip select 0 output	**GPIO11**		PU	Input
H5		LCD_CS1#	IO	Serial display interface chip select 1 output	**GPIO12**		PU	Input
SIM Card Interface								
J2		**SIMRST**	O	SIM card reset output				0
J3		**SIMCLK**	O	SIM card clock output				0
J4		**SIMVCC**	O	SIM card supply power control				0
K1		**SIMSEL**	O	SIM card supply power select				0
K1		**SIMDATA**	IO	SIM card data input/output				0

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Dedicated GPIO Interface								
K3		**GPIO13**	IO	General purpose input/output 13			PD	Input
K4		**GPIO14**	IO	General purpose input/output 14			PD	Input
K5		**GPIO15**	IO	General purpose input/output 15			PD	Input
Miscellaneous								
L2		**SYSRST#**	I	System reset input active low				Input
L3		**WATCHDOG#**	O	Watchdog reset output				
M1		**SRCLKENAN**	O	External TCXO enable active low	GPO1			0
N1		**SRCLKENA**	O	External TCXO enable active high	GPO2			1
Keypad Interface								
M3		**KCOL4**	I	Keypad column 4			PU	Input
M2		**KCOL3**	I	Keypad column 3			PU	Input
P1		**KCOL2**	I	Keypad column 2			PU	Input
N2		**KCOL1**	I	Keypad column 1			PU	Input
P2		**KCOL0**	I	Keypad column 0			PU	Input
N3		**KROW4**	O	Keypad row 4				0
L4		**KROW3**	O	Keypad row 3				0
M4		**KROW2**	O	Keypad row 2				0
K5		**KROW1**	O	Keypad row 1				0
L5		**KROW0**	O	Keypad row 0				0
Alerter Interface								
P5		**ALERTER**	O	Pulse width modulated signal for buzzer	GPO3			0
External Interrupt Interface								
N5		**EINT0**	I	External interrupt 0			PU	Input
M5		**EINT1**	I	External interrupt 1			PU	Input
K6		**EINT2**	I	External interrupt 2	nIRQ		PU	Input
External Memory Interface								
L6		**ED0**	IO	External memory data bus 0				Input
K7		**ED1**	IO	External memory data bus 1				Input
L7		**ED2**	IO	External memory data bus 2				Input
P7		**ED3**	IO	External memory data bus 3				Input
N7		**ED4**	IO	External memory data bus 4				Input
M7		**ED5**	IO	External memory data bus 5				Input
M8		**ED6**	IO	External memory data bus 6				Input
N8		**ED7**	IO	External memory data bus 7				Input
L8		**ED8**	IO	External memory data bus 8				Input
K8		**ED9**	IO	External memory data bus 9				Input
L9		**ED10**	IO	External memory data bus 10				Input

P9		**ED11**	IO	External memory data bus 11				Input
M9		**ED12**	IO	External memory data bus 12				Input
K9		**ED13**	IO	External memory data bus 13				Input
M10		**ED14**	IO	External memory data bus 14				Input
N10		**ED15**	IO	External memory data bus 15				Input
L10		**ERD#**	O	External memory read strobe				1
K10		**EWR#**	O	External memory write strobe				1
N6		**ELCDWR#**	O	External LCD controller write strobe				1
M11		**ECS0#**	O	External memory chip select 0				1
L11		**ECS1#**	O	External memory chip select 1				1
P12		**ECS2#**	O	External memory chip select 2				1
M6		**ECS3#**	O	External memory chip select 3				1
P13		**ELB#**	O	External memory lower byte strobe				1
N13		**EUB#**	O	External memory upper byte strobe				1
P14		**EA0**	O	External memory address bus 0				0
M13		**EA1**	O	External memory address bus 1				0
M12		**EA2**	O	External memory address bus 2				0
M14		**EA3**	O	External memory address bus 3				0
L12		**EA4**	O	External memory address bus 4				0
L13		**EA5**	O	External memory address bus 5				0
L14		**EA6**	O	External memory address bus 6				0
J10		**EA7**	O	External memory address bus 7				0
K11		**EA8**	O	External memory address bus 8				0
K12		**EA9**	O	External memory address bus 9				0
K14		**EA10**	O	External memory address bus 10				0
J11		**EA11**	O	External memory address bus 11				0
J12		**EA12**	O	External memory address bus 12				0
J13		**EA13**	O	External memory address bus 13				0
H10		**EA14**	O	External memory address bus 14				0
H11		**EA15**	O	External memory address bus 15				0
H13		**EA16**	O	External memory address bus 16				0
H12		**EA17**	O	External memory address bus 17				0
H14		**EA18**	O	External memory address bus 18				0
G14		**EA19**	O	External memory address bus 19				0
G12		**EA20**	O	External memory address bus 20				0
G13		**EA21**	O	External memory address bus 21				0
G11		**EA22**	IO	External memory address bus 22	GPO0	XLCDE		0
F12		**EA23**	O	External memory address bus 23				0
UARTInterface								

G10		**URXD1**	I	UART 1 receive data			PU	Input
F11		**UTXD1**	O	UART 1 transmit data				1
F10		**UCTS1**	I	UART 1 clear to send			PU	Input
E12		**URTS1**	O	UART 1 request to send				1
E14		UCTS2	IO	UART 2 clear to send	**GPIO17**	UDSR1	PU	Input
E13		URTS2	IO	UART 2 request to send	**GPIO18**	UDTR1	PU	Input
E11		URXD2	IO	UART 2 receive data	**GPIO19**		PU	Input
E10		UTXD2	IO	UART 2 transmit data	**GPIO20**		PU	Input
D12		UREF_CK	IO	UART1 external reference clock for high speed download	**GPIO21**	nFIQ	PU	Input
Digital Audio Interface								
D11		DAICLK	IO	DAI clock output	**GPIO0**	**BOOT**	PD	Input
C14		DAIPCMOUT	IO	DAI pcm data out	**GPIO1**	**MSIZE**	PD	Input
C13		DAIPCMIN	IO	DAI pcm data input	**GPIO2**		PU	Input
B14		DAIRST	IO	DAI reset signal input	**GPIO3**		PU	Input
Analog Interface								
B13		**AU_OUT1_P**		Earphone 1 amplifier output (+)				
A14		**AU_OUT1_N**		Earphone 1 amplifier output (-)				
B12		**AU_OUT0_N**		Earphone 0 amplifier output (-)				
A13		**AU_OUT0_P**		Earphone 0 amplifier output (+)				
C11		**AU_MICBIAS_P**		Microphone bias supply (+)				
B11		**AU_MICBIAS_N**		Microphone bias supply (-)				
E9		**AU_VREF_N**		Audio reference voltage (-)				
D10		**AU_VREF_P**		Audio reference voltage (+)				
B10		**AU_VIN0_P**		Microphone 0 amplifier input (+)				
A10		**AU_VIN0_N**		Microphone 0 amplifier input (-)				
D9		**AU_VIN1_N**		Microphone 1 amplifier input (-)				
C9		**AU_VIN1_P**		Microphone 1 amplifier input (+)				
D8		**BDLAQP**		Quadrature input (Q+) baseband codec downlink				
C8		**BDLAQN**		Quadrature input (Q-) baseband codec downlink				
A8		**BDLAIN**		In-phase input (I+) baseband codec downlink				
B8		**BDLAIP**		In-phase input (I-) baseband codec downlink				
B7		**BUPAIP**		In-phase output (I+) baseband codec uplink				
A7		**BUPAIN**		In-phase output (I-) baseband codec uplink				
C7		**BUPAQN**		Quadrature output (Q+) baseband codec				

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				uplink				
D7		**BUPAQP**		Quadrature output (Q-) baseband codec uplink				
B6		**APC**		Automatic power control DAC output				
D6		**AUXADIN0**		Auxiliary ADC input 0				
E6		**AUXADIN1**		Auxiliary ADC input 1				
C5		**AUXADIN2**		Auxiliary ADC input 2				
A5		**AUXADIN3**		Auxiliary ADC input 3				
B5		**AUXADIN4**		Auxiliary ADC input 4				
D5		**AUX_REF**		Auxiliary ADC reference voltage input				
A4		**AFC**		Automatic frequency control DAC output				
E5		**AFC_BYP**		Automatic frequency control DAC bypass capacitance				
VCXO Interface								
C4		**SYSCLK**		13MHz or 26MHz system clock input				
RTC Interface								
B3		**XIN**		32.768 KHz crystal input				
A2		**XOUT**		32.768 KHz crystal output				
B2		**BBWAKEUP**	O	Baseband power on/off control				1
Supply Voltages								
F1		**VDDK**		Supply voltage of internal logic				
P4		**VDDK**		Supply voltage of internal logic				
P11		**VDDK**		Supply voltage of internal logic				
F14		**VDDK**		Supply voltage of internal logic				
F2		**VSSK**		Ground of internal logic				
N4		**VSSK**		Ground of internal logic				
N11		**VSSK**		Ground of internal logic				
F13		**VSSK**		Ground of internal logic				
P8		**VDD33_EMI**		Supply voltage of memory interface driver				
P10		**VDD33_EMI**		Supply voltage of memory interface driver				
N14		**VDD33_EMI**		Supply voltage of memory interface driver				
J14		**VDD33_EMI**		Supply voltage of memory interface driver				
N9		**VSS33_EMI**		Ground of memory interface driver				
N12		**VSS33_EMI**		Ground of memory interface driver				
K13		**VSS33_EMI**		Ground of memory interface driver				
D1		**VDD33**		Supply voltage of drivers except memory interface				

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J1		**VDD33**		Supply voltage of drivers except memory interface				
P3		**VDD33**		Supply voltage of drivers except memory interface				
D14		**VDD33**		Supply voltage of drivers except memory interface				
B1		**VSS33**		Ground of drivers except memory interface				
G1		**VSS33**		Ground of drivers except memory interface				
L1		**VSS33**		Ground of drivers except memory interface				
P6		**VSS33**		Ground of drivers except memory interface				
D13		**VSS33**		Ground of drivers except memory interface				
B4		**AVDD_PLL**		Supply voltage for PLL				
D4		**AVSS_PLL**		Ground for PLL supply				
A3		**AVDD_RTC**		Supply voltage for Real Time Clock				
Analog Supplies								
C12		**AVDD_BUF**		Supply voltage for voice band transmit section				
A12		**AVSS_BUF**		GND for voice band transmit section				
A11		**AVDD_AFE**		Supply voltage for voice band receive section				
C10		**AGND_AFE**		GND reference voltage for voice band section				
B9		**AVSS_AFE**		GND for voice band receive section				
A9		**AGND_RFE**		GND reference voltage for baseband section, APC, AFC and AUXADC				
E8		**AVSS_GSMRFTX**		GND for baseband transmit section				
C6		**AVDD_GSMRFTX**		Supply voltage for baseband transmit section				
E7		**AVSS_RFE**		GND for baseband receive section, APC, AFC and AUXADC				
A6		**AVDD_RFE**		Supply voltage for baseband receive section, APC, AFC and AUXADC				

Table 2 Pin Descriptions (**Bolded** types are functions at reset)

2.3 Power Description

Ball 12X12	Ball 10X10	Name	IO Supply	IO GND	Core Supply	Core GND	Remark
B1		**VSS33**					
C2		JTRST#	VDD33	VSS33	VDDK	VSSK	
C3		JTCK			VDDK	VSSK	
A1		JTDI			VDDK	VSSK	
C1		JTMS			VDDK	VSSK	
D3		JTDO			VDDK	VSSK	
D2		BPI_BUS0			VDDK	VSSK	
F5		BPI_BUS1			VDDK	VSSK	
E4		BPI_BUS2			VDDK	VSSK	
D1		**VDD33**					Typ. 2.8V
E2		BPI_BUS3	VDD33	VSS33	VDDK	VSSK	
E3		BPI_BUS4			VDDK	VSSK	
E1		BPI_BUS5			VDDK	VSSK	
F2		**VSSK**					
F4		BPI_BUS6	VDD33	VSS33	VDDK	VSSK	
F1		**VDDK**					Typ. 1.8V
F3		BPI_BUS7	VDD33	VSS33	VDDK	VSSK	
G5		BSI_CS0			VDDK	VSSK	
G4		BSI_DATA			VDDK	VSSK	
G3		BSI_CLK			VDDK	VSSK	
G1		**VSS33**					
G2		PWM	VDD33	VSS33	VDDK	VSSK	
H1		LCD_DATA			VDDK	VSSK	
H3		LCD_A0			VDDK	VSSK	
H2		LCD_CLK			VDDK	VSSK	
H4		LCD_CS0#			VDDK	VSSK	
H5		LCD_CS1#			VDDK	VSSK	
J2		SIMRST			VDDK	VSSK	
J3		SIMCLK			VDDK	VSSK	
J1		**VDD33**					Typ. 2.8V
J4		SIMVCC	VDD33	VSS33	VDDK	VSSK	
K1		SIMSEL			VDDK	VSSK	
K1		SIMDATA			VDDK	VSSK	
K3		GPIO13			VDDK	VSSK	
K4		GPIO14			VDDK	VSSK	

K5		GPIO15			VDDK	VSSK	
L2		SYSRST_B			VDDK	VSSK	
L3		WATCHDOG#			VDDK	VSSK	
L1		**VSS33**					
M1		SRCLKENAN	VDD33	VSS33	VDDK	VSSK	
N1		SRCLKENA			VDDK	VSSK	
M3		KCOL4			VDDK	VSSK	
M2		KCOL3			VDDK	VSSK	
P1		KCOL2			VDDK	VSSK	
N2		KCOL1			VDDK	VSSK	
P2		KCOL0			VDDK	VSSK	
N3		KROW4			VDDK	VSSK	
P3		**VDD33**					Typ. 2.8V
L4		KROW3	VDD33	VSS33	VDDK	VSSK	
M4		KROW2			VDDK	VSSK	
K5		KROW1			VDDK	VSSK	
N4		**VSSK**					
L5		KROW0	VDD33	VSS33	VDDK	VSSK	
P4		**VDDK**					Typ. 1.8V
P5		ALERTER	VDD33	VSS33	VDDK	VSSK	
N5		EINT0			VDDK	VSSK	
M5		EINT1			VDDK	VSSK	
K6		EINT2			VDDK	VSSK	
P6		**VSS33**			VDDK	VSSK	
M6		ECS3#	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
N6		ELCDWR#			VDDK	VSSK	
L6		ED0			VDDK	VSSK	
K7		ED1			VDDK	VSSK	
L7		ED2			VDDK	VSSK	
P7		ED3			VDDK	VSSK	
N7		ED4			VDDK	VSSK	
P8		**VDD33_EMI**					Typ. 1.8V/2.8V
M7		ED5	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
M8		ED6			VDDK	VSSK	
N8		ED7			VDDK	VSSK	
L8		ED8			VDDK	VSSK	
K8		ED9			VDDK	VSSK	
N9		**VSS33_EMI**					
L9		ED10	VDD33_EMI	VSS33_EMI	VDDK	VSSK	

P9		ED11			VDDK	VSSK	
M9		ED12			VDDK	VSSK	
K9		ED13			VDDK	VSSK	
M10		ED14			VDDK	VSSK	
P10		**VDD33_EMI**					Typ. 1.8V/2.8V
N10		ED15	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
N11		**VSSK**					
L10		ERD#	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
P11		**VDDK**					Typ. 1.8V
K10		EWR#	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
M11		ECS0#			VDDK	VSSK	
N12		**VSS33_EMI**					
L11		ECS1#	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
P12		ECS2#			VDDK	VSSK	
P13		ELB#			VDDK	VSSK	
N13		EUB#			VDDK	VSSK	
N14		**VDD33_EMI**					Typ. 1.8V/2.8V
P14		EA0	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
M13		EA1			VDDK	VSSK	
M12		EA2			VDDK	VSSK	
M14		EA3			VDDK	VSSK	
L12		EA4			VDDK	VSSK	
L13		EA5			VDDK	VSSK	
L14		EA6			VDDK	VSSK	
K13		**VSS33_EMI**					
J10		EA7	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
K11		EA8			VDDK	VSSK	
K12		EA9			VDDK	VSSK	
K14		EA10			VDDK	VSSK	
J11		EA11			VDDK	VSSK	
J12		EA12			VDDK	VSSK	
J13		EA13			VDDK	VSSK	
H10		EA14			VDDK	VSSK	
J14		**VDD33_EMI**					Typ. 1.8V/2.8V
H11		EA15	VDD33_EMI	VSS33_EMI	VDDK	VSSK	
H13		EA16			VDDK	VSSK	
H12		EA17			VDDK	VSSK	
H14		EA18			VDDK	VSSK	
G14		EA19			VDDK	VSSK	

G12		EA20			VDDK	VSSK	
G13		EA21			VDDK	VSSK	
G11		EA22			VDDK	VSSK	
F12		EA23					
F13		**VSSK**					
G10		URXD1	VDD33	VSS33	VDDK	VSSK	
F14		**VDDK**					Typ. 2.8V
F11		UTXD1			VDDK	VSSK	
F10		UCTS1			VDDK	VSSK	
E12		URTS1	VDD33	VSS33	VDDK	VSSK	
E14		UCTS2			VDDK	VSSK	
E13		URTS2			VDDK	VSSK	
D14		**VDD33**					Typ. 2.8V
E11		URXD2	VDD33	VSS33	VDDK	VSSK	
D13		**VSS33**					
E10		UTXD2			VDDK	VSSK	
D12		UREF_CK			VDDK	VSSK	
D11		DAICLK			VDDK	VSSK	
C14		DAIPCMOUT	VDD33	VSS33	VDDK	VSSK	
C13		DAIPCMIN			VDDK	VSSK	
B14		DAIRST			VDDK	VSSK	
F9		TESTMODE			VDDK	VSSK	
B13		AU_OUT1_P					
A14		AU_OUT1_N					
B12		AU_OUT0_N					
C12		**AVDD_BUF**					Typ. 2.8V
A13		AU_OUT0_P					
A12		**AVSS_BUF**					
C11		AU_MICBIAS_P					
B11		AU_MICBIAS_N					
A11		**AVDD_AFE**					Typ. 2.8V
E9		AU_VREF_N					
D10		AU_VREF_P					
C10		**AGND_AFE**					
B10		AU_VIN0_P					
A10		AU_VIN0_N					
D9		AU_VIN1_N					
C9		AU_VIN1_P					
B9		**AVSS_AFE**					

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D8		BDLAQP					
C8		BDLAQN					
A9		**AGND_RFE**					
A8		BDLAIN					
B8		BDLAIP					
E8		**AVSS_GSMRFTX**					
B7		BUPAIP					
A7		BUPAIN					
C6		**AVDD_GSMRFTX**					Typ. 2.8V
C7		BUPAQN					
D7		BUPAQP					
E7		**AVSS_RFE**					
B6		APC					
A6		**AVDD_RFE**					Typ. 2.8V
D6		AUXADIN0					
E6		AUXADIN1					
C5		AUXADIN2					
A5		AUXADIN3					
B5		AUXADIN4					
D5		AUX_REF					
A4		AFC					
E5		AFC_BYP					
B4		**AVDD_PLL**					Typ. 2.8V
C4		SYSCLK	AVDD_PLL	AVSS_PLL	AVDD_PLL	AVSS_PLL	
D4		**AVSS_PLL**					
A3		**AVDD_RTC**					Typ. 1.5V
B3		XIN	AVDD_RTC	AVSS_RTC	AVDD_RTC	AVSS_RTC	
A2		XOUT			AVDD_RTC	AVSS_RTC	
B2		BBWAKEUP			AVDD_RTC	AVSS_RTC	
B1		**AVSS_RTC**					

Table 3 Power Descriptions

3 Micro-Controller Unit Subsystem

Figure 5 illustrates the block diagram of the Micro-Controller Unit Subsystem in MT6205B. A 32-bit RISC processor, the ARM7TDMI, plays the role of the major bus master in controlling the whole subsystem. Essentially, it communicates with all the other on-chip modules by way of system buses: AHB Bus and APB Bus.

All bus transactions originate from bus masters, while slaves can only respond requests from bus masters. Prior to a data transfer can be established, bus master must ask for bus ownership. This is accomplished by request-grant handshaking protocol between masters and Arbiter.

Two levels of bus hierarchy are designed to provide alternatives for different performance requirements, i.e. AHB Bus and APB Bus for system back bone and peripheral buses, respectively. To have high performance and proper efficiency, the AHB Bus provides 32-bit data path with multiplex scheme for bus interconnections.

For APB Bus, it supports 16-bit addressing and both 16-bit and 32-bit data paths. Since it is designated to have reduced interface complexity for lower data transfer rate, it is isolated from high bandwidth AHB Bus by APB Bridge. APB Bus is also optimized for minimal power consumption by employing gated clock scheme.

Whenever the target slave is resided on AHB Bus, the transaction is conducted directly on AHB Bus. However, if the target slave is a peripheral, the transaction should be further forwarded to APB Bus by APB Bridge.

Only memory addressing method is used in MT6205B based system. All components are mapped onto MCU 32-bit address space. A Memory Management Unit is employed to have a central decode scheme. It generates certain selection signals for each memory-addressed modules on AHB Bus.

In order to off-load the processor core some times, a DMA Controller is designated to act as a master and commence the bus resources on AHB Bus of doing fast data movement between modules. This controller integrates two DMA channels.

The Interrupt Controller provides a software interface to manipulate interrupt events . It can handle up to 16 interrupt sources asserted at the same time. In general, it generates 2 levels of interrupt requests to the processor.

A 32K Byte SRAM is provided for acting as system memory for high-speed data access. For factory programming purpose, a Boot ROM module is used. These two modules use the same Internal Memory Controller to connect to AHB Bus.

External Memory Interface supports both 8-bit and 16-bit devices. Since AHB Bus is 32-bit wide, all the data transfer will be converted into several 8-bit or 16-bit cycles depending on the data width of target device. Note that, this interface is specific to asynchronous components, like Flash, SRAM and parallel LCD. This interface supports also page mode type of Flash.

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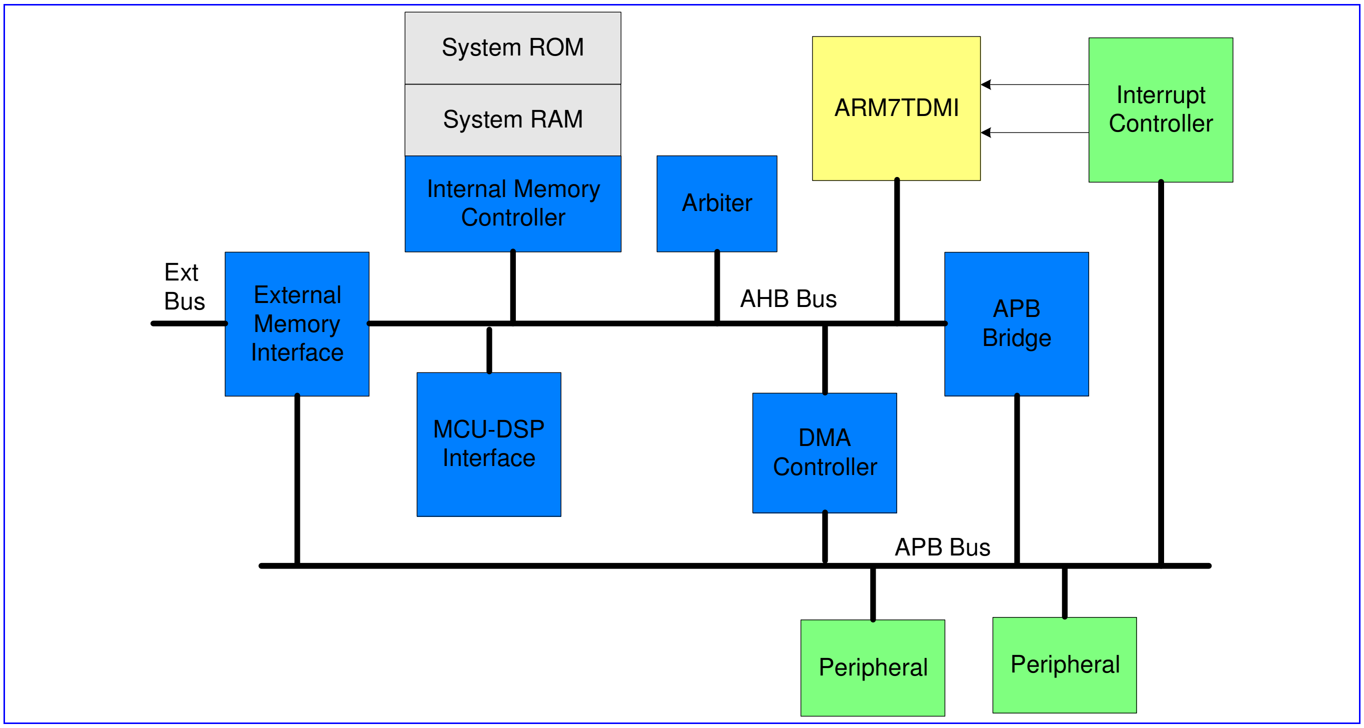

Figure 5 Block Diagram of the Micro-Controller Unit Subsystem in MT6205B

3.1 Processor Core

3.1.1 General Description

The Micro-Controller Unit Subsystem in MT6205B is built up with a 32-bit RISC core, ARM7TDMI that is based on Von Neumann architecture with a single 32-bit data bus carrying both instructions and data. To adapt to the AMBA based system, there designs a high efficiency master interface connecting the processor core and the AHB Bus. It incorporates numbers of functions necessary in high performance and low power operations including:

- Address and Data Pipelining
- Low Latency Bus Interface to Achieve 1 CPI (Cycle Per Instruction) Performance
- Processor Sleep Mode

3.2 Memory Management

3.2.1 General Description

The processor core of MT6205B, ARM7TDMI, supports only memory addressing method for instruction fetch and data access. It manages a 32-bit address space that has addressing capability up to 4GB. System RAM, System ROM, Registers, MCU Peripherals and external components are all mapped onto such 32-bit address space, as depicted in **Figure 6**.

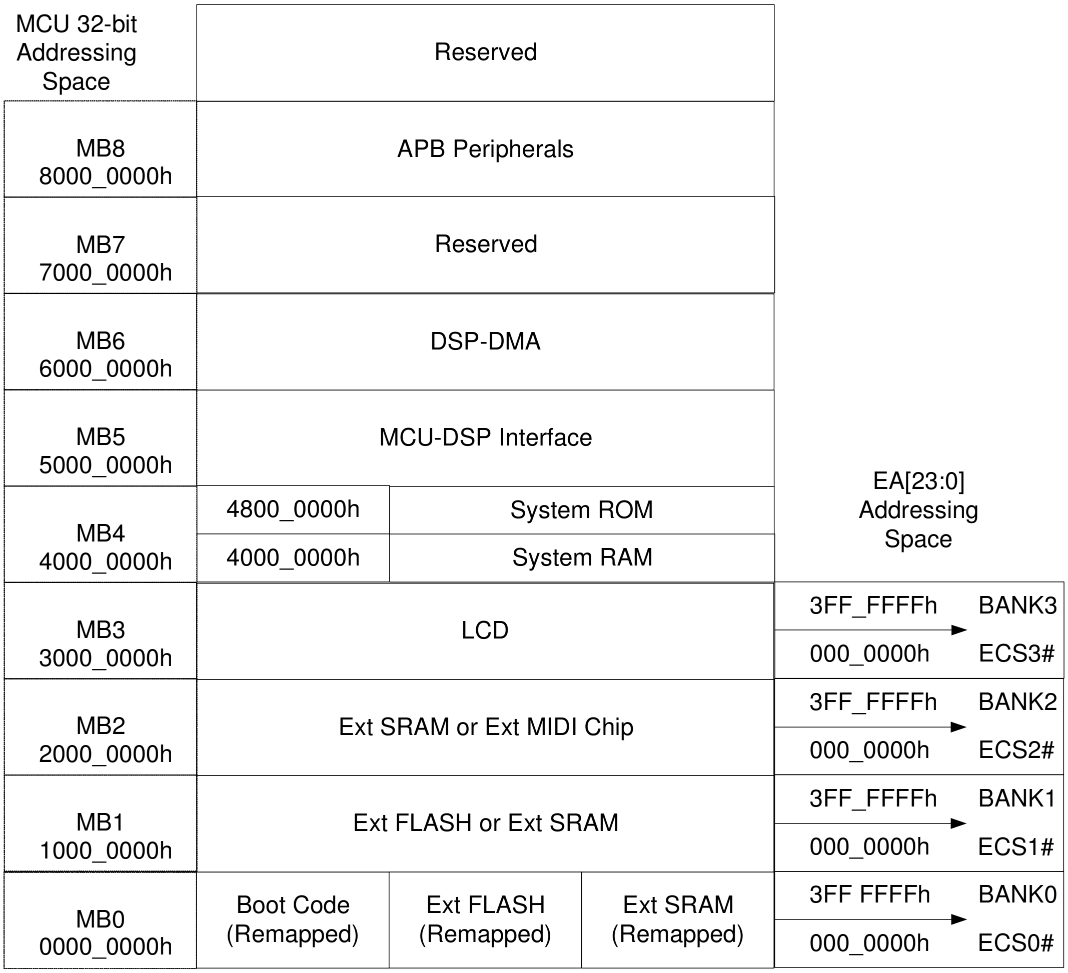

Figure 6 The Memory Layout of MT6205B

The address space is organized as basis of blocks with size of 256M Bytes for each. Memory blocks MB0-MB8 are determined and currently dedicated to specific functions, as shown in **Table 4**, while the others are reserved for future usage. Essentially, the block number is uniquely selected by address line A31-A28 of internal system bus.

Memory Block	Block Address A31-A28	Address Range	Description
MB0	0h	00000000h-0FFFFFFFh	Boot Code or EXT Flash or EXT SRAM
MB1	1h	10000000h-1FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB2	2h	20000000h-2FFFFFFFh	EXT SRAM or EXT MIDI
MB3	3h	30000000h-3FFFFFFFh	LCD
MB4	4h	40000000h-47FFFFFFh	System RAM
		48000000h-4FFFFFFFh	System ROM
MB5	5h	50000000h-5FFFFFFFh	MCU-DSP Share RAM Interface
MB6	6h	60000000h-6FFFFFFFh	DSP-DMA

MB7	7h	70000000h-7FFFFFFFh	Reserved
MB8	8h	80000000h-8FFFFFFFh	APB Slaves

Table 4 Definitions of Memory Blocks in MT6205B

3.2.1.1 External Access

To have external access, the MT6205B outputs 24 bits (A23-A0) of address lines together with 4 selection signals that correspond to associate memory blocks. That is, MT6205B can support at most 4 MCU addressable external components at the same time. The data width of internal system bus is fixed as 32-bit wide, while the data width of the external components can be either 8 or 16 bit.

Since devices are usually available with variety operating grades, adaptive configurations for different applications are needed. MT6205B provides software programmable registers to be configured to adapt operating conditions in terms of different wait-states. Descriptions will be detailed in 3.7 External Memory Interface.

3.2.1.2 Memory Re-mapping Mechanism

To permit system being configured with more flexible, a memory re-mapping mechanism is provided. It allows software program to swap BANK0 (ECS0#) and BANK1 (ECS1#) dynamically. Whenever the bit value of RM0 in register EMI_REMAP is changed, these two banks will be swapped accordingly. Besides, it also permits system being boot in different sequence as detailed in 3.2.1.3 Boot Sequence.

3.2.1.3 Boot Sequence

Since the ARM7TDMI core always starts to fetch instructions from the lowest memory address at 00000000h (MB0) after system being reset. It is designed to have a dynamic mapping architecture capable of associating Boot Code, external Flash or external SRAM with memory block MB0.

By default, the Boot Code is mapped onto MB0 while the state of BOOT pin is “0”. But, this configuration can be changed by altering the state of BOOT pin before system reset or programming bit value of RM1 in register EMI_REMAP directly.

MT6205B system provides two kinds of boot up scheme:

- Start up system of running codes from Boot Code for factory programming
- Start up system of running codes from external FLASH or ROM device for normal operation

3.2.1.3.1 Boot Code

The Boot Code is placed with Memory Re-Mapping Mechanism in External Memory Controller and includes just two words of instructions as shown below. It is quite obvious that there is a jump instruction that leads the processor to run the code started at address of 48000000h where the System ROM is placed.

```
ADDRESS      BINARY CODE    ASSEMBLY
00000000h    E51FF004h      LDR PC, 0x4
00000004h    48000000h      (DATA)
```

3.2.1.3.2 Factory Programming

The configuration for factory programming is shown in **Figure 7**. Usually the Factory Programming Host connects with MT6205B by way of UART1 interface. To have it works properly, the system should boot up from Boot Code. That is the BOOT pin should be tied to GND. The down load speed can be up to 230K bps while MCU is running at 13MHz.

After system being reset, the Boot Code will guide the processor to run the Factory Programming software placed in System ROM. Then, MT6205B will start and continue to poll the UART1 port until valid information is detected. The first information received on the UART1 will be used to configure the chip for factory programming. The Flash down loader program is then transferred into System RAM or external SRAM.

Further information will be detailed in MT6205B Software Programming Specification.

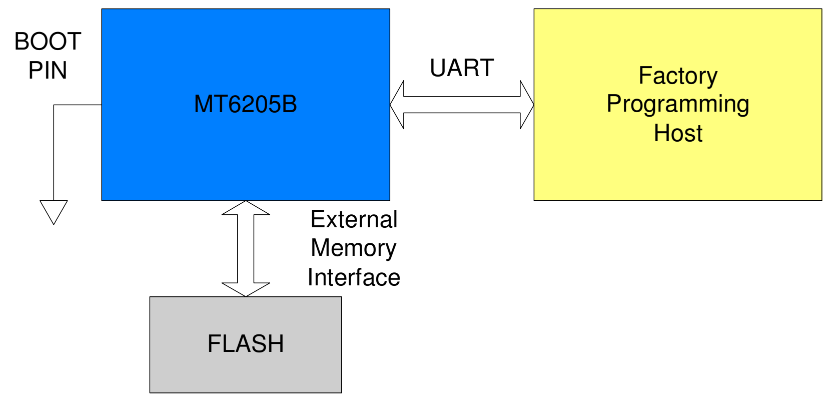

Figure 7 System configuration required for factory programming

3.2.1.4 Little Endian Mode

The MT6205B system always treats 32-bit words of memory in Little Endian format. In Little Endian mode, the lowest numbered byte in a word is stored in the least significant byte, and the highest numbered byte in the most significant position. Byte 0 of the memory system is therefore connected to data lines 7 through 0.

3.3 Bus System

3.3.1 General Description

Two levels of bus hierarchy are employed in constructing the Micro-Controller Unit Subsystem of MT6205B. As depicted in **Figure 5**, AHB Bus and APB Bus serve for system backbone and peripheral buses, while an APB bridge connects these two buses. Both AHB and APB Buses operate at the same clock rate as processor core.

The APB Bridge is the only bus master resided on the APB bus. All APB slaves are mapped onto memory block MB8 in MCU 32-bit addressing space. A central address decoder is implemented inside the bridge to generate those select signals for individual peripheral. In addition, since the base address of each APB slave has been associated to select signals, the address bus on APB will contains only the value of offset address.

The maximum address space that can be allocated to a single APB slave is 32KB, i.e. 16-bit address lines. The width of data bus is mainly constrained to 16-bit to minimize the design complexity and power consumption while some of them

uses 32-bit data bus to accommodate more bandwidth. In the case where an APB slave needs large amount of transfers, the device driver can also request a DMA resource or channel to conduct a burst of data transfer. The base address and data width of each peripheral are listed in **Table 5**.

Base Address	Description	Data Width	Software Base ID
8000_0000h	Configuration Registers (Clock, Power Down, Version and Reset)	16	CONFG Base
8001_0000h	External Memory Interface	16	EMI Base
8002_0000h	Interrupt Controller	16	CIRQ Base
8003_0000h	DMA Controller	16	DMA Base
8004_0000h	Reset Generation Unit	16	RGU Base
8005_0000h	Reserved		
8006_0000h	Reserved		
8010_0000h	General Purpose Timer	16	GPT Base
8011_0000h	Keypad Scanner	16	KP Base
8012_0000h	General Purpose Inputs/Outputs	16	GPIO Base
8013_0000h	UART 1	16	UART1 Base
8014_0000h	SIM Interface	16	SIM Base
8015_0000h	Pulse-Width Modulation Outputs	16	PWM Base
8016_0000h	Alerter Interface	16	ALTER Base
8017_0000h	LCD Interface	16	LCD Base
8018_0000h	UART 2	16	UART2 Base
8020_0000h	TDMA Timer	16	TDMA Base
8021_0000h	Real Time Clock	16	RTC Base
8022_0000h	Base-Band Serial Interface	32	BSI Base
8023_0000h	Base-Band Parallel Interface	16	BPI Base
8024_0000h	Automatic Frequency Control Unit	16	AFC Base
8025_0000h	Automatic Power Control Unit	32	APC Base
8026_0000h	Reserved		
8027_0000h	Auxiliary ADC Unit	16	AUXADC Base
8028_0000h	Divider/Modulus Coprocessor	32	DIVIDER Base
8029_0000h	CSD Accelerator	32	CSD_ACC Base
8030_0000h	MCU-DSP Shared Register	16	SHARE Base
8031_0000h	DSP Patch Unit	16	PATCH Base
8040_0000h	Audio Front End	16	AFE Base
8041_0000h	Base-Band Front End	16	BFE Base

Table 5 Register Base Addresses for MCU Peripherals

REGISTER ADDRESS	REGISTER NAME	SYNONYM
CONFG + 0000h	Hardware Version Register	HW_VER

CONFG + 0004h	Firmware Version Register	FW_VER
CONFG + 0008h	Hardware Code Register	HW_CODE
CONFG + 0400h	AHB Bus Control Register	AHB_CON
CONFG + 0404h	APB Bus Control Register	APB_CON

Table 6 APB Bridge Register Map

3.3.2 Register Definitions

CONFG+0000h Hardware Version Register HW_VERSION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXTP				MAJREV				MINREV				HFIX			
Type	R				R				R				R			
Reset	8				B				0				0			

This register is useful for software program to determine the hardware version of the chip. It will have a new value whenever each metal fix or major step is performed. All these values are incremented by a step of 1.

HFIX Iteration to fix a hardware bug, in case of some layer mask fixed

MINREV Minor Revision of the chip, in case of all layer masks changed

MAJREV Major Revision of the chip

EXTP This field shows the existence of Hardware Code Register that presents the Hardware ID while the value is other than zero.

CONFG+0004h Firmware Version Register FW_VERSION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXTP				MAJREV				MINREV				FFIX			
Type	R				R				R				R			
Reset	8				B				0				0			

This register is useful for software program to determine the Firmware ROM version that is included in this chip. All these values are incremented by a step of 1.

FFIX Iteration to fix a firmware bug

MINREV Minor Revision of the firmware

MAJREV Major Revision of the firmware

EXTP This field shows the existence of Hardware Code Register that presents the Hardware ID when the value is other than zero.

CONFG+0008h Hardware Code Register HW_CODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CODE3				CODE2				CODE1				CODE0			
Type	R				R				R				R			
Reset	6				2				0				5			

This register presents the Hardware ID.

CODE This version of chip is coded as 6205h.

CONFG+0400h AHB Bus Control Register AHB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCUP
Type																R/W
Reset																0

This register is used to control the activities on AHB Bus.

MCUP MCU Protection Mode

While DMA channel is enabled, the processor core and DMA master share the AHB Bus evenly. In other word, the execution time for process core may be varied time to time. For timing critical application, this timing variant may cause failure. To prevent this happing, this bit is used to raise the priority of processor core to highest on AHB Bus whenever it is set to “1”.

0 Normal Mode

1 MCU Protection Mode

CONFG+0404h APB Bus Control Register APB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				APBW4	APBW3	APBW2	APBW1	APBW0				APBR4	APBR3	APBR2	APBR1	APBR0
Type				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0				1	1	1	1	1

This register is used to control the timing of Read Cycle and Write Cycle on APB Bus.

APBR0-APBR4 Read Access Time on APB Bus

0 1-Cycle Access

1 2-Cycle Access

APBW0-APBW4 Write Access Time on APB Bus

0 1-Cycle Access

1 2-Cycle Access

3.4 Direct Memory Access

3.4.1 General Description

A generic DMA Controller placed on AHB Bus supports fast data transfers while also off-loading the processor. With this controller, specific devices on AHB or APB buses can benefit greatly from quickly completing data movement from or to memory module, i.e. Internal System RAM or External SRAM. Such Generic DMA Controller can also be used to connect any two devices other than memory module as long as they can be addressed in memory space. Currently, 3 major specific data transfer paths are provided in MT6205B, as shown in **Figure 8**:

- UART from/to Memory
- SIM from/to Memory
- DSP-DMA from/to Memory

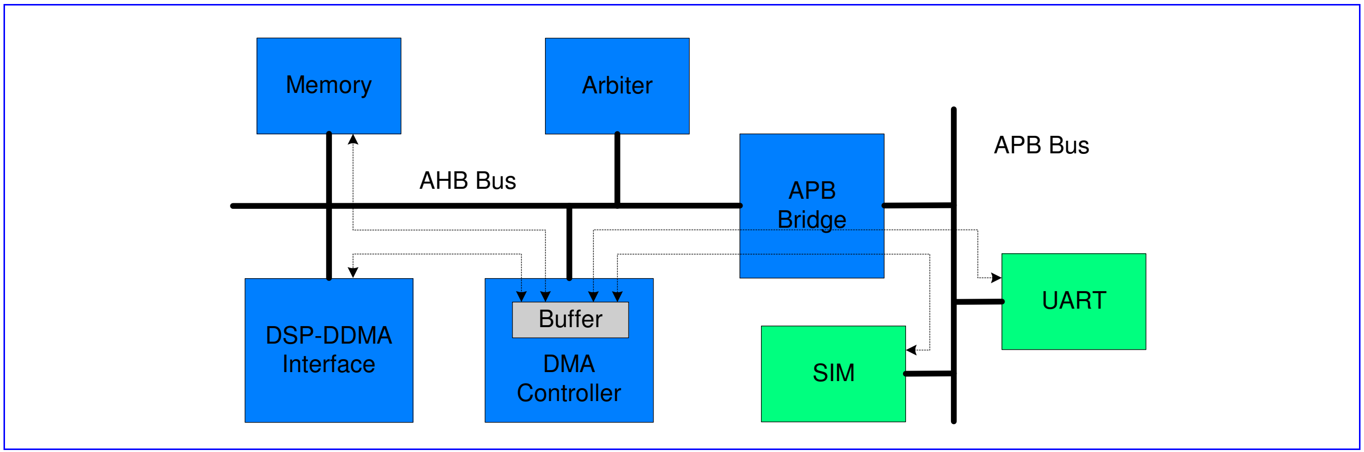

Figure 8 Variety Data Paths of DMA Transfers

Only two channels of data transfer are supported at one time. Each channel has the similar set of registers to configure to different scheme as desired. If more than two devices are requesting the DMA resources at the same time, software based arbitration should be employed. Once the service candidate is decided, the responsible device driver should configure the Generic DMA Controller properly in order to conduct DMA transfers. Both Interrupt and Polling based schemes in handling the completion event are supported. The block diagram of such generic DMA Controller is illustrated in **Figure 9**.

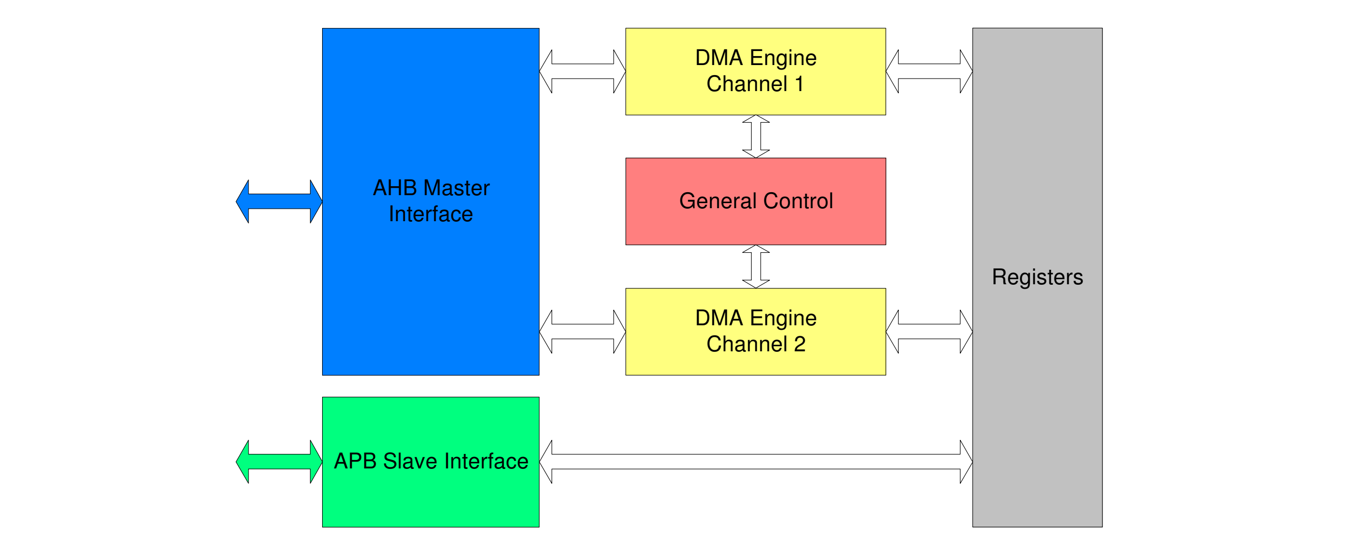

Figure 9 Block Diagram of Direct memory Access Module

REGISTER ADDRESS	REGISTER NAME	SYNONYM
DMA + 0000h	DMA Global Status Register	DMA_GLBSTA
DMA + 0004h	DMA Channel 1 MSB Source Address Register	DMA1_MSBSRC
DMA + 0008h	DMA Channel 1 LSB Source Address Register	DMA1_LSBSRC
DMA + 000Ch	DMA Channel 1 MSB Destination Address Register	DMA1_MSBDST
DMA + 0010h	DMA Channel 1 LSB Destination Address Register	DMA1_LSBDST
DMA + 0014h	DMA Channel 1 Transfer Count Register	DMA1_COUNT
DMA + 0018h	DMA Channel 1 Control Register	DMA1_CON

DMA + 001Ch	DMA Channel 1 Start Register	DMA1_START
DMA + 0020h	DMA Channel 1 Interrupt Status Register	DMA1_INTSTA
DMA + 0024h	DMA Channel 1 Interrupt Acknowledge Register	DMA1_ACKINT
DMA + 0104h	DMA Channel 2 MSB Source Address Register	DMA2_MSBSRC
DMA + 0108h	DMA Channel 2 LSB Source Address Register	DMA2_LSBSRC
DMA + 010Ch	DMA Channel 2 MSB Destination Address Register	DMA2_MSBDST
DMA + 0110h	DMA Channel 2 LSB Destination Address Register	DMA2_LSBDST
DMA + 0114h	DMA Channel 2 Transfer Count Register	DMA2_COUNT
DMA + 0118h	DMA Channel 2 Control Register	DMA2_CON
DMA + 011Ch	DMA Channel 2 Start Register	DMA2_START
DMA + 0120h	DMA Channel 2 Interrupt Status Register	DMA2_INTSTA
DMA + 0124h	DMA Channel 2 Interrupt Acknowledge Register	DMA2_ACKINT

Table 7 DMA Controller Register Map

3.4.2 Register Definitions

DMA+0000h DMA Global Status Register DMA_GLBSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IT2	RUN2			IT1	RUN1
Type											R	R			R	R
Reset											0	0			0	0

This register helps software program being well aware of the global status of both DMA channels.

RUN1 DMA channel 1 status
- **0** Channel 1 is stopped or has completed the transfer already.
- **1** Channel 1 is currently running.

IT1 Interrupt status for channel 1
- **0** No interrupt is generated.
- **1** An interrupt is pending and waiting for service.

RUN2 DMA channel 2 status
- **0** Channel 1 is stopped or has completed the transfer already.
- **1** Channel 1 is currently running.

IT2 Interrupt status for channel 2
- **0** No interrupt is generated.
- **1** An interrupt is pending and waiting for service.

DMA+0004h DMA Channel 1 MSB Source Address Register DMA1_MSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[31:16]															
Type	R/W															
Reset	0															

DMA+0008h DMA Channel 1 LSB Source Address Register DMA1_LSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[15:0]															
Type	R/W															
Reset	0															

DMA+0104h DMA Channel 2 MSB Source Address Register DMA2_MSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[31:16]															
Type	R/W															
Reset	0															

DMA+0108h DMA Channel 2 LSB Source Address Register DMA2_LSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[15:0]															
Type	R/W															
Reset	0															

The above registers once being used will be in pair to prompt the base or current address that a DMA channel is dealing with currently, i.e. both MSB and LSB parts always being considered unitedly as one set. In regard to a write to this set, it specifies the base address of transfer source for a DMA channel. Before being able to program these registers, the software program should be sure of that STR in DMAn_START is set to '0', that is the DAM channel is stopped and disabled completely. Other wise, the DMA channel may run out of order. In regard to a read to this set, it shows the value exactly the same as the one being written while SINC in DMAn_CON is set to "0". With SINC being set to "1", it appears the current source address that the data being getting from. It allows software program being well tracking the progress of DMA transfer.

SRC **SRC**[31:0] specifies the base or current address of transfer source for a DMA channel, i.e. channel 1 or 2.

WRITE base address of transfer source

READ base address of transfer source if SINC in DMAn_CON is "0"

current address of transfer source if SINC in DMAn_CON is "1"

DMA+000Ch DMA Channel 1 MSB Destination Address Register DMA1_MSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[31:16]															
Type	R/W															
Reset	0															

DMA+0010h DMA Channel 1 LSB Destination Address Register DMA1_LSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[15:0]															
Type	R/W															
Reset	0															

DMA+010Ch DMA Channel 2 MSB Destination Address Register DMA2_MSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[31:16]															

Type	R/W
Reset	0

DMA+0110h DMA Channel 2 LSB Destination Address Register DMA2_LSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[15:0]															
Type	R/W															
Reset	0															

The above registers once being used should be in pair to index the base or current address that a DMA channel is dealing with currently, i.e. both MSB and LSB parts always being considered unitedly as one set. In regard to a write to this set, it specifies the base address of the transfer destination for a DMA channel. Before being able to program these register, the software should be sure of that STR in DMAn_START is set to ‘0’, that is the DAM channel is stopped and disabled completely. Other wise, the DMA channel may run out of order. In regard to a read to this set, it shows the value exactly the same as the one being written while DINC in DMAn_CON is set to “0”. With DINC being set to “1”, it appears the current destination address that the data being sending to. It allows software program being well tracking the progress of DMA transfer.

DST **DST**[31:0] specifies the base or current address of transfer destination for a DMA channel, i.e. channel 1 or 2.

WRITE base address of transfer destination

READ base address of transfer destination if DINC in DMAn_CON is “0”
current address of transfer destination if DINC in DMAn_CON is “1”

DMA+0014h DMA Channel 1 Transfer Count Register DMA1_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	R/W															
Reset	0															

DMA+0114h DMA Channel 2 Transfer Count Register DMA2_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	R/W															
Reset	0															

This register specifies the amount of total transfer count that the DMA channel is required to perform. Upon completion, the DMA channel generates an interrupt request to the processor while ITEN in DMAn_CON is set as ‘1’. Note that the total size of data being transferred by a DMA channel is determined by LEN together with the SIZE in DMAn_CON, i.e. LEN x SIZE.

LEN The amount of total transfer count

DMA+0018h DMA Channel 1 Control Register DMA1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITEN		CYCLE					TMOD		MAS		DRQ	DINC	SINC	SIZE	
Type	R/W		R/W					R/W		R/W		R/W	R/W	R/W	R/W	
Reset	0		0					0		0		0	0	0	0	

DMA+0118h DMA Channel 2 Control Register DMA2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITEN		CYCLE					TMOD		MAS		DRQ	DINC	SINC	SIZE	
Type	R/W		R/W					R/W		R/W		R/W	R/W	R/W	R/W	
Reset	0		0					0		0		0	0	0	0	

This register appeals all the available control schemes for a DMA channel that is readily for software program to configure with. Note that all these fields cannot be changed while DMA transfer is in progress or unexpected situation may occur.

SIZE Data size within the confine of a bus cycle per transfer
These bits confines the size to the specified value for individual bus cycle that data is moving between source and destination. The size is in terms of byte and has maximum value of 4 bytes. It is mainly decided by the data width of a DMA master.
- **00** Byte transfer/1 byte
- **01** Half-word transfer/2 bytes
- **10** Word transfer/4 bytes
- **11** Reserved

SINC Appearance control for the source address registers DMAn_MSBSRC and DMAn_LSBSRC
- **0** The base address of the source
- **1** The current address of the source that the DMA channel is currently dealing with.

DINC Appearance control for the destination address registers DMAn_MSBDST and DMAn_LSBDST
- **0** The base address of the destination
- **1** The current address of the destination that the DMA channel is currently dealing with

DREQ Throttle and handshake control for DMA transfer
- **0** No throttle control during DMA transfer or transfers occurred only between memories
- **1** Hardware handshake management
  The DMA master is able to throttle down the transfer rate by way of request-grant handshake.

MAS Selection of DMA master
To specify the desired DMA Master, the DRQ should be set to 1.
- **00** Reserved
- **01** Channel 1: UART1 Write/Rx, Channel 2: UART1 Read/Tx
- **10** Channel 1: UART2 Read/Tx, Channel 2: UART2 Write/Rx
- **11** SIM

TMOD Transfer mode
- **0** Single mode
  Single data transfer is performed per bus handshake.
- **1** Burst mode
  Multiple data transfers are performed in a burst per bus handshake. The amount of data transfers each burst is determined by CYCLE.

CYCLE The amount of data transfers per bus handshake

ITEN Interrupt generation upon DMA transfer being completed
- **0** No interrupt request is generated
- **1** Generate interrupt request

DMA+001Ch DMA Channel 1 Start Register DMA1_START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	R/W															
Reset	0															

DMA+011Ch DMA Channel 2 Start Register DMA2_START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	R/W															
Reset	0															

This register controls the activity of a DMA channel. Note that prior to set STR to “1”, all the configurations should be done by giving proper value to the registers including DMAn_MSBSRC, DMAn_LSBSRC, DMAn_MSBDST, DMAn_LSBDST, DMAn_COUNT and DMAn_CON. Note also that once the STR is set to “1”, the hardware will not clear it automatically no matter the DMA channel accomplishes the DMA transfer or not. Put another way, the value of **STR** keeps as “1” in spite of the completion of DMA transfer. Therefore, the software program should be sure to clear **STR** to “0” before being able to re-start another DMA transfer.

STR Start control for a DMA channel

- **0** The DMA channel is stopped
- **1** The DMA channel is started and running

DMA+0020h DMA Channel 1 Interrupt Status Register DMA1_INTSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT															
Type	R															
Reset	0															

DMA+0120h DMA Channel 2 Interrupt Status Register DMA2_INTSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT															
Type	R															
Reset	0															

This register shows the interrupt status of a DMA channel. In fact the value is exactly the same as in DMA_GLBSTA.

INT Interrupt Status for DMA Channel

- **0** No interrupt request is generated.
- **1** One interrupt request is pending and waiting for service

DMA+0024h DMA Channel 1 Interrupt Acknowledge Register DMA1_ACKINT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK															
Type	W															
Reset	0															

DMA+0124h DMA Channel 2 Interrupt Acknowledge Register DMA2_ACKINT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK															
Type	W															
Reset	0															

This register is used to acknowledge the current interrupt request associated with the completion event of a DMA channel by software program. Note that this is a write-only register, any read to it will return a value of "0".

ACK Interrupt acknowledge for the DMA channel

- **0** No effect
- **1** Interrupt request is acknowledged and should be relinquished.

3.5 Interrupt Controller

3.5.1 General Description

Figure 10 outlines the major functionality of the MCU Interrupt Controller. The interrupt controller processes all interrupt sources coming from external lines and internal MCU peripherals. Since ARM7TDMI core supports two levels of interrupt latency, this controller will generate two request signals: nFIQ for fast, low latency interrupt request and nIRQ for more general interrupts with lower priority.

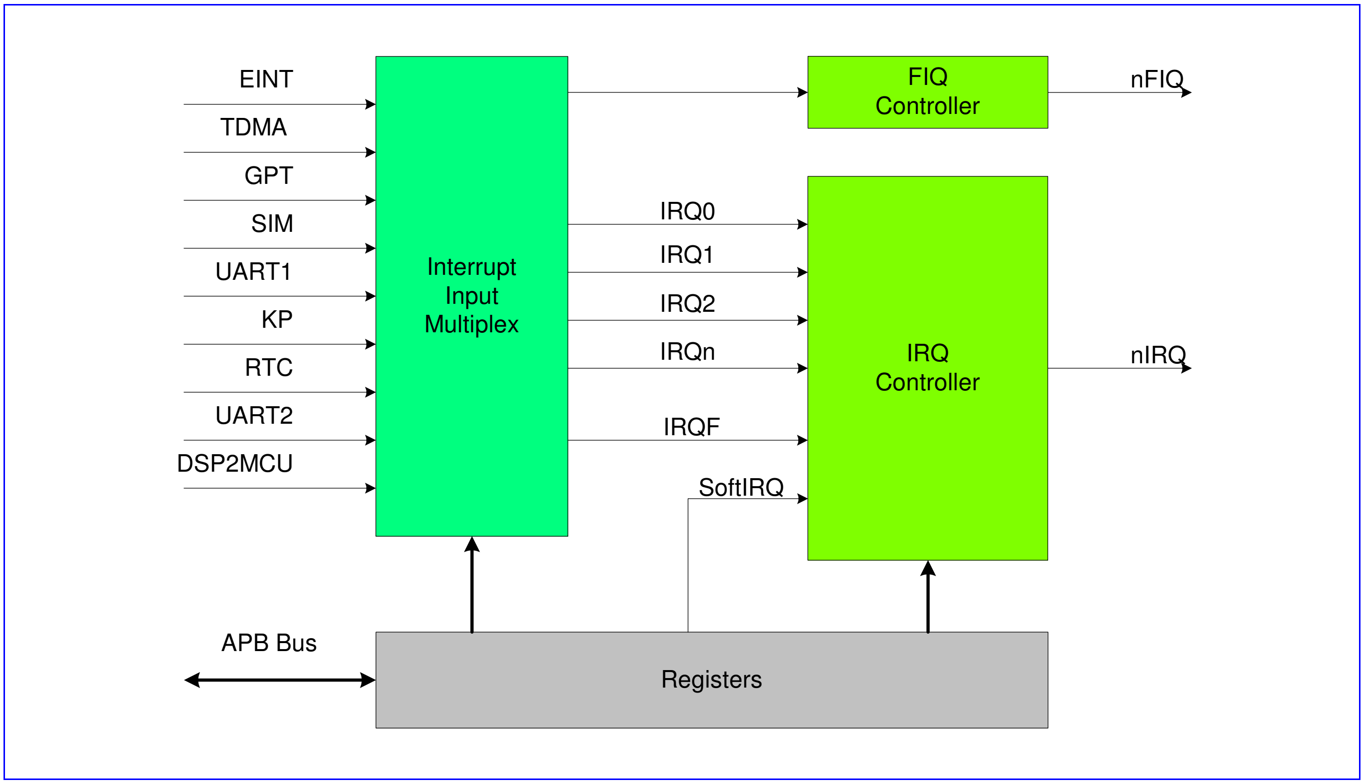

Figure 10 Block Diagram of the Interrupt Controller

One and only one of the interrupt sources can be assigned to FIQ Controller and have the highest priority in requesting timing critical service. All the others should share the same nIRQ signal by connecting them to IRQ Controller. The IRQ Controller manages up 16 interrupt lines of IRQ0 to IRQF with fixed priority in descending order.

The Interrupt Controller provides a simple software interface by mean of registers to manipulate the interrupt request shared system. IRQ Selection Registers and FIQ Selection Register determine the source priority and connecting relation among sources and interrupt lines. IRQ Source Status Register allows software program to identify the source of interrupt that generates the interrupt request. IRQ Mask Register provides software to mask out undesired sources some time. End of Interrupt Register permits software program to indicate the controller that a certain interrupt service routine has been finished.

Binary coded version of IRQ Source Status Register is also made available for software program to helpfully identify the interrupt source. Note that while taking this advantage, it should also take the binary coded version of End of Interrupt Register coincidently.

The essential Interrupt Table of ARM7TDMI core is shown as **Table 8**.

Address	Description
00000000h	System Reset
00000018h	IRQ
0000001Ch	FIQ

Table 8 Interrupt Table of ARM7TDMI

3.5.1.1 External Interrupt

This interrupt controller also integrates an External Interrupt Controller that can support up to 3 interrupt requests coming from external sources as shown in **Figure 11**. Those external interrupts can be used for different kind of applications, mainly for event detections: detection of hand free connection, detection of hood opening, detection of battery charger connection.

Since the external event may be unstable in a certain period, de-bounce mechanism is included to ensure the functionality. The circuitry is mainly used to verify that if the input signal remains stable for a programmable number of periods of the clock. When this condition is satisfied, for the appearance or the disappearance of the input, the output of the de-bounce logic will change to the desired state. Note that, because it uses the 32KHz slow clock for doing de-bounce process, the parameters takes effect no sooner than 1 32KHz clock cycle, ~31.25us, after software program sets them.

Note also that this External Interrupt Controller handles only level sensitive type of interrupt sources.

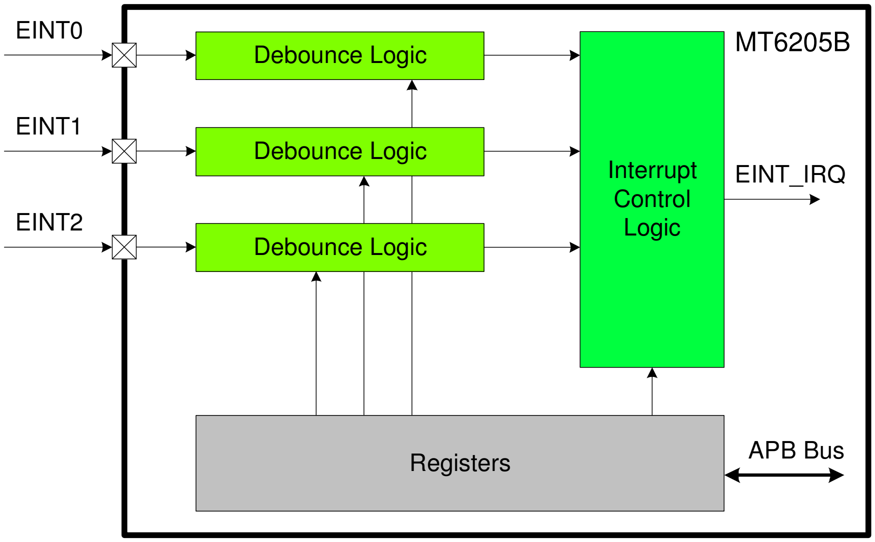

Figure 11 Block diagram of External Interrupt Controller

REGISTER ADDRESS	REGISTER NAME	SYNONYM
CIRQ + 0000h	IRQ Selection 0 Register	IRQ_SEL0
CIRQ + 0004h	IRQ Selection 1 Register	IRQ_SEL1
CIRQ + 0008h	IRQ Selection 2 Register	IRQ_SEL2
CIRQ + 000Ch	IRQ Selection 3 Register	IRQ_SEL3
CIRQ + 0010h	FIQ Selection Register	FIQ_SEL
CIRQ + 0014h	IRQ Mask Register	IRQ_MASK
CIRQ + 0018h	IRQ Status Register	IRQ_STA
CIRQ + 001Ch	IRQ End of Interrupt Register	IRQ_EOI
CIRQ + 0020h	IRQ Sensitive Register	IRQ_SENS
CIRQ + 0024h	IRQ Software Interrupt Register	IRQ_SOFT
CIRQ + 0028h	FIQ Control Register	FIQ_CON
CIRQ + 002Ch	FIQ End of Interrupt Register	FIQ_EOI
CIRQ + 0038h	Binary Coded Value of IRQ_STATUS	IRQ_STA2
CIRQ + 003Ch	Binary Coded Value of IRQ_EOI	IRQ_EOI2
CIRQ + 0040h	EINT Status Register	EINT_STA
CIRQ + 0044h	EINT Mask Register	EINT_MASK
CIRQ + 0048h	EINT Interrupt Acknowledge Register	EINT_INTACK
CIRQ + 0050h	EINT0 De-bounce Control Register	EINT0_CON
CIRQ + 0060h	EINT1 De-bounce Control Register	EINT1_CON
CIRQ + 0070h	EINT2 De-bounce Control Register	EINT2_CON
CIRQ + 00A0h	Clear Control for IRQ Mask Register	IRQ_MASK_CLR
CIRQ + 00A4h	Set Control for IRQ Mask Register	IRQ_MASK_SET

CIRQ + 00A8h	Clear Control for EINT Mask Register	EINT_MASK_CLR
CIRQ + 00ACh	Set Control for EINT Mask Register	EINT_MASK_SET

Table 9 Interrupt Controller Register Map

3.5.2 Register Definitions

CIRQ+0000h IRQ Selection 0 Register IRQ_SEL0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ3				IRQ2				IRQ1				IRQ0			
Type	R/W				R/W				R/W				R/W			
Reset	3				2				1				0			

CIRQ+0004h IRQ Selection 1 Register IRQ_SEL1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ7				IRQ6				IRQ5				IRQ4			
Type	R/W				R/W				R/W				R/W			
Reset	7				6				5				4			

CIRQ+0008h IRQ Selection 2 Register IRQ_SEL2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQB				IRQA				IRQ9				IRQ8			
Type	R/W				R/W				R/W				R/W			
Reset	B				A				9				8			

CIRQ+000Ch IRQ Selection 3 Register IRQ_SEL3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF				IRQE				IRQD				IRQC			
Type	R/W				R/W				R/W				R/W			
Reset	F				E				D				C			

CIRQ+0010h FIQ Selection Register FIQ_SEL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIQ			
Type													R/W			
Reset													0			

The IRQ/FIQ Selection Registers provide system designers with a flexible routing scheme to make various mappings of priority among interrupt sources possible. It allows the interrupt sources being mapped onto interrupt requests of either nFIQ or nIRQ. Where only one interrupt source can be assigned to FIQ, the other ones should share IRQ by mapping them onto IRQ0 to IRQE connected to IRQ controller. The priority of IRQ0-IRQF is fixed, i.e. IRQ0 > IRQ1 > IRQ2 > … > IRQD > IRQF. During the software configuration process, the Interrupt Source Code of desired interrupt source should be written into source field of the corresponding IRQ_SEL0-IRQ_SEL3/FIQ_SEL. 4-bit Interrupt Source Codes for all interrupt sources are fixed and defined in **Table 10**.

Interrupt Source	Interrupt Source Code
TDMA_CTIRQ1	0000

TDMA_CTIRQ2	0001
UART1	0010
RTC	0011
LCD	0100
SIM	0101
DSP2CPU	0110
KP	0111
Reserved	1000
GPT	1001
EINT	1010
DMA	1011
TDMA	1100
UART2	1101
EINT2	1110
EXT_NIRQ	1111

Table 10 Interrupt Source Code for Interrupt Sources

FIQ, IRQ0-F The 4-bit content of this field would be the Interrupt Source Code shown in **Table 10** indicating that the certain interrupt source uses the associated interrupt line to generate interrupt requests.

CIRQ+0014h IRQ Mask Register IRQ_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register contains mask bit for each interrupt line in IRQ Controller. It allows each interrupt source of IRQ0 to IRQF to be disabled or masked out separately under software control. After System Reset, all bit values will be set to ‘1’ to indicate that interrupt requests are prohibited.

IRQ0-F Mask Control for the Associated Interrupt Source in IRQ Controller

- **0** Interrupt is enabled
- **1** Interrupt is disabled

CIRQ+0018h IRQ Source Status Register IRQ_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This Register allows software to poll which interrupt line generates the nIRQ interrupt request. A bit set to ‘1’ indicates a corresponding active interrupt line. Only one flag is active at a time. Any reads to it clears the active bit and de-asserts nIRQ signal. The IRQ_STA is type of READ-ONLY, write access will be no effect to the content.

IRQ0-F Interrupt Indication for the Associated Interrupt Source

- **0** The associated interrupt source is non-active

1 The associated interrupt source is asserted

CIRQ+001Ch IRQ End of Interrupt Register IRQ_EOI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register provides a mean for software to relinquish and refresh the Interrupt Controller. Writing a '1' to the specific bit position will result in an End of Interrupt Command internally to the corresponding interrupt line.

IRQ0-F End of Interrupt Command for the Associated Interrupt Line

0 No service is currently in progress or pending

1 Interrupt request is in-service

CIRQ+0020h IRQ Sensitive Register IRQ_SENS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

All interrupt lines of IRQ Controller, IRQ0-IRQF can be programmed as either edge or level sensitive. By default, all the interrupt lines are edge sensitive and should be active LOW. For edge sensitive interrupt line, while being activated, the output of edge-detection circuitry will remain HIGH until after the MCU acknowledges the interrupt by issuing End of Interrupt command and then being able to enable further interrupts to occur. For level sensitive interrupt lines, the interrupt source should be cleared before EOI command of writing IRQ_EOI in preventing another interrupt to occur.

IRQ0-F Sensitive Type of the Associated Interrupt Source

0 Edge sensitivity with active LOW

1 Level sensitivity with active LOW

CIRQ+0024h IRQ Software Interrupt Register IRQ_SOFT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Setting "1" to the specific bit position generates a software interrupt for corresponding Interrupt Line before mask. This register is used for debug purpose.

IRQ0-IRQF Software Interrupt

CIRQ+0028h FIQ Control Register FIQ_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SENS	MASK
Type															R/W	R/W
Reset															0	1

This register provides a mean for software program to control the FIQ Controller.

MASK Mask Control for the FIQ Interrupt Source

0 Interrupt is enabled

1 Interrupt is disabled

SENS Sensitive Type of the FIQ Interrupt Source

0 Edge sensitivity with active LOW

1 Level sensitivity with active LOW

CIRQ+002Ch FIQ End of Interrupt Register FIQ_EOI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EOI
Type																W
Reset																0

This register provides a mean for software to relinquish and refresh the FIQ Controller. Writing a '1' to the specific bit position will result in an End of Interrupt Command internally to the corresponding interrupt line.

EOI End of Interrupt Command

CIRQ+0038h Binary Coded Value of IRQ_STATUS IRQ_STA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													STS			
Type													R			
Reset													0			

This Register is a binary coded version of IRQ_STA. It is used for software program to poll which interrupt line generates the nIRQ interrupt request in much more easy way. Any read to it makes the same result of as reading IRQ_STA. The IRQ_STA2 is also type of READ-ONLY, write access takes no effect to the content. Note that, IRQ_STA2 should be coupled with IRQ_EOI2 while using it.

STS Binary Coded Value of IRQ_STA

CIRQ+003Ch Binary Coded Value of IRQ_EOI IRQ_EOI2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EOI			
Type													W			
Reset													0			

This register is a binary coded version of IRQ_EOI. It provides a more easy way for software program to relinquish and refresh the Interrupt Controller. Writing a specific code will result an End of Interrupt Command internally to the corresponding interrupt line. Note that, IRQ_EOI2 should be coupled with IRQ_STA2 while using it.

EOI Binary Coded Value of IRQ_EOI

CIRQ+0040h EINT Interrupt Status Register EINT_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EINT2	EINT1	EINT0
Type														R	R	R
Reset														0	0	0

This register keeps up with current status that which EINT Source generates the interrupt request.

EINT0-EINT3 Interrupt Status

0 No Interrupt Request is generated

1 Interrupt Request is pending

CIRQ+0044h EINT Interrupt Mask Register EINT_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EINT2	EINT1	EINT0
Type														R/W	R/W	R/W
Reset														1	1	1

This register controls that if EINT Source is allowed to generate interrupt request. Setting a "1" to the specific bit position prohibits the External Interrupt Line to active accordingly.

EINT0-EINT3 Interrupt Mask

- **0** Interrupt Request is enabled
- **1** Interrupt Request is disabled

CIRQ+0048h EINT Interrupt Acknowledge Register EINT_INTACK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EINT2	EINT1	EINT0
Type														W	W	W
Reset														0	0	0

Writing "1" to the specific bit position means to acknowledge the interrupt request correspondingly to the External Interrupt Line source.

EINT0-EINT3 Interrupt Acknowledge

- **0** No effect
- **1** Interrupt Request is acknowledged

CIRQ+0050h EINT0 De-bounce Control Register EINT0_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN				POL	CNT										
Type	R/W				R/W	R/W										
Reset	0				0	0										

CIRQ+0060h EINT1 De-bounce Control Register EINT1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN				POL	CNT										
Type	R/W				R/W	R/W										
Reset	0				0	0										

CIRQ+0070h EINT2 De-bounce Control Register EINT2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN				POL	CNT										
Type	R/W				R/W	R/W										
Reset	0				0	0										

These registers control the de-bounce logic for external interrupt sources in order to minimize the possibility of false activations.

CNT De-bounce Duration in terms of numbers of 32KHz clock cycles

POL Activation Type of the EINT Source

- **0** Negative polarity

1 Positive polarity

EN De-bounce Control Circuit

0 Disable

1 Enable

CIRQ+00A0h Clear Control for IRQ Mask Register IRQ_MASK_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

CIRQ+00A8h Clear Control for EINT Interrupt Mask Register EINT_MASK_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EINT2	EINT1	EINT0
Type														WC	WC	WC

Clear control for IRQ Mask Register and EINT Interrupt Mask Register. When software program writes a “1” to the specific bit position, it causes the corresponding bit of Mask Register to be cleared to “0”. While the other bits remain unchanged, if their values are specified as “0”.

CIRQ+00A4h Set Control for IRQ Mask Register IRQ_MASK_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS

CIRQ+00ACh Set Control for EINT Interrupt Mask Register EINT_MASK_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EINT2	EINT1	EINT0
Type														WS	WS	WS

Set control for IRQ Mask Register and EINT Interrupt Mask Register. When software program writes a “1” to the specific bit position, it causes the corresponding bit of Mask Register to be set to “1”. While the other bits remain unchanged, if their values are specified as “0”.

3.6 Internal Memory Controller

3.6.1 General Description

3.6.2 System RAM

MT6205B provides a 32K Byte size of on-chip memory module acting as System RAM for data access with zero latency. Such module is composed of a high speed synchronous SRAM with AHB Slave Interface connected to system backbone AHB Bus, as shown in **Figure 12**. The synchronous SRAM operates at the same clock as AHB Bus and is organized as 32-bit wide with 4 byte-write signals capable for byte operations.

3.6.3 System ROM

The System ROM is primarily used to store software program for Factory Programming. However, due to it's advantageous zero latency performance, some of timing critical codes are also placed in this area. This module is composed of high-speed diffusion ROM with AHB Slave Interface connected to system backbone AHB Bus, as shown in **Figure 12**. It operates at the same clock as AHB Bus and is organized as 32-bit wide.

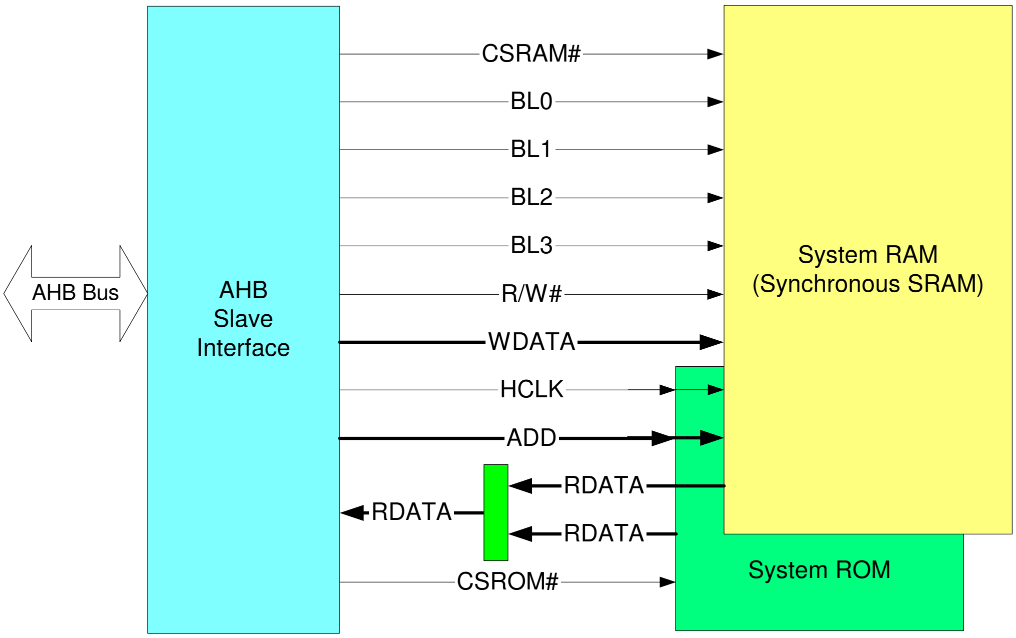

Figure 12 Block Diagram of Internal Memory Controller

3.7 External Memory Interface

3.7.1 General Description

MT6205B incorporates a powerful and flexible memory controller, External Memory Interface, to connect with a variety of memory components. This controller provides generic access schemes to asynchronous type of memory devices, such as Flash and SRAM. It can simultaneously support up to 4 memory banks BANK0-BANK3 with maximum size of 16MB each.

Since most of the target asynchronous components have similar AC requirements, it is desirable to have a generic configurable scheme to interface them. Such that, software program can treat different components by simply specifying certain predefined parameters. All those parameters are based on cycle time of 13MHz.The interface definition based on such asynchronous scheme is listed in **Table 11**. Note that, this interface always operates data in Little Endian format for all type of accesses.

Page mode Flash is supported for those applications required to run EIP (execution in place).

Signal Name	Type	Description

EA[23:0]	O	Address Bus
ED[15:0]	I/O	Data Bus
EWR#	O	Write Enable Strobe
ERD#	O	Read Enable Strobe
ELB#	O	Lower Byte Strobe
EUB#	O	Upper Byte Strobe
ECS0#	O	BANK0 Selection Signal
ECS1#	O	BANK1 Selection Signal
ECS2#	O	BANK2 Selection Signal
ECS3#	O	BANK3 Selection Signal
ELCD_WR#	O	Write Enable Strobe for LCD Module with Color Acceleration

Table 11 **External Memory Interface of MT6205B for Asynchronous Type Components**

This controller can also handle parallel type of LCD. By connecting with them, both 6800 and 8080 types of control method are supported. The interface definition is detailed in **Table 12**. To have the capability of color acceleration, the alternative configuration is shown in **Table 13**.

Bus Type \ Signal Name	ECS3#	EA[23]	ERD#	EWR#	ED[15:0]	LCDE
6800 series	CS#	A0/RS	-	R/W#	D[n:0]	E
8080 series	CS#	A0/RS	RD#	WR#	D[n:0]	-

Table 12 General Configuration for Parallel LCD Interface

Bus Type \ Signal Name	ECS3#	EA[23]	EA[22]	ELCD_WR#	ED[15:0]	LCDE
6800 series	CS#	A0/RS	-	R/W#	D[n:0]	E
8080 series	CS#	A0/RS	RD#	WR#	D[n:0]	-

Table 13 Configuration for Parallel LCD Interface with Color Acceleration

REGISTER ADDRESS	REGISTER NAME	SYNONYM
EMI + 0000h	EMI Control Register 0 (BANK0)	EMI_CON0
EMI + 0004h	EMI Control Register 1 (BANK1)	EMI_CON1
EMI + 0008h	EMI Control Register 2 (BANK2)	EMI_CON2
EMI + 000Ch	EMI Control Register 3 (BANK3)	EMI_CON3
EMI + 0010h	EMI Re-map Control Register	EMI_REMAP
EMI + 0014h	EMI General Control Register	EMI_GEN
EMI + 0030h	Code Cache and Code Prefetch Control Register	PREFETCH_CON

Table 14 External Memory Interface Register Map

MediaTek Inc. Confidential

3.7.2 Register Definitions

EMI+0000h EMI Control Register 0 EMI_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	CSE	WST					PSIZE	PRLT	PMODE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	MSIZE	1	0	0					0	0	0	7				

EMI+0004h EMI Control Register 1 EMI_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	CSE	WST					PSIZE	PRLT	PMODE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0008h EMI Control Register 2 EMI_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	CSE	WST					PSIZE	PRLT	PMODE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+000Ch EMI Control Register 3 EMI_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	CSE	WST					PSIZE	PRLT	PMODE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

For each bank (BANK0-BANK3), there is a dedicate control register in connection with the associated bank controller. These registers have the timing parameters that help the controller to convey memory access into proper timing waveform. Note that, Except for parameter DW that is in unit of bit, all the other parameters specified explicitly are based on bus clock speed in terms of cycle count.

RLT Read Latency Time

Specifying the parameter RLT turns effectively to insert wait-states in bus transfer to requesting agent. Such parameter should be chosen carefully to meet the common parameter tACC (access time) for device in read operation. Example is shown below.

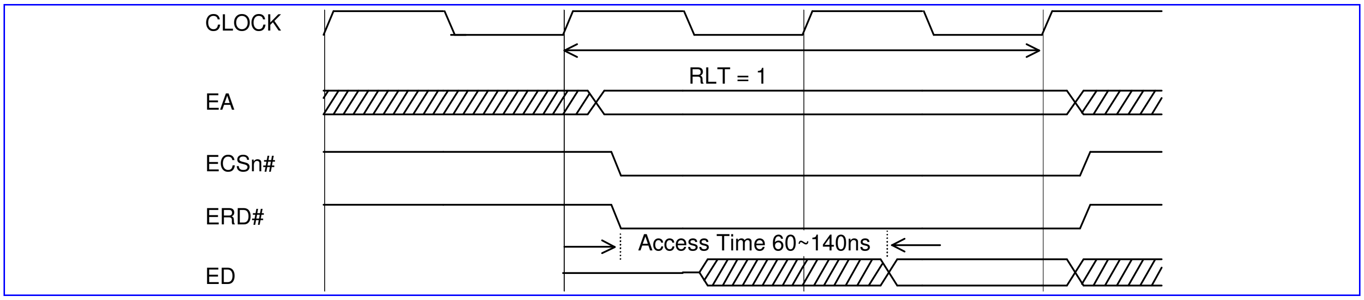

Figure 13 One Wait State Read Timing Diagram

Access Time	Read Latency Time
< 60ns	0
60ns ~ 140ns	1
140ns ~ 215ns	2

Table 15 Reference value of Read Latency Time for variant memory devices

PMODE Page Mode Control

If target device supports page mode operations, the Page Mode Control can be enabled. Read in Page Mode is determined by set of parameters: PRLT and PSIZE.

0 disable page mode operation

1 enable page mode operation

PRLT Read Latency Within the Same Page

Since page mode operation only help to eliminate read latency in subsequent burst within the same page, it doesn't matter with the initial latency at all. Thus, it should still adopt RLT parameter for initial read or burst read between different pages though PMODE is set "1".

0 zero wait state

1 one wait state

Page Access Time	Read Latency Time
< 60ns	0
60ns ~ 140ns	1

Table 16 Reference value of Read Latency Within the Same Page for variant page type memory devices

PSIZE Page Size for Page Mode Operation

These bit positions describe the page size that the Page Mode enabled device will behave. The size is specified in two cases.

0 8 bytes, EA[23:3] remains the same

1 16 bytes, EA[23:4] remains the same

WST Write Wait State

Specifying the parameters to extend adequate setup and hold time for target component in write operation. Those parameters also effectively insert wait-states in bus transfer to requesting agent. Example is shown in **Figure 14** and Table 17.

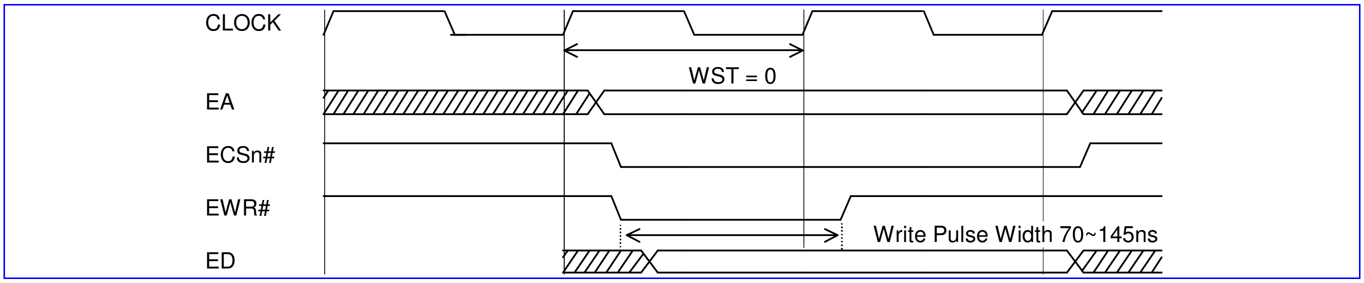

Figure 14 Zero Wait State Write Timing Diagram

Write Pulse Width (Write Data Setup Time)	Write Wait State
< 70ns	0
70ns ~ 145ns	1
145ns ~ 220ns	2

Table 17 Reference value of Write Wait State for variant memory devices

LCD Control Type for Parallel LCD Interface

0 8080 series based

1 6800 series based

CSE Chip Select to Command Delay

0 No delay

1 With 1T delay

DW Data Width

Since the data width of internal system bus is fixed as 32-bit wide, any access to external components might be converted into more than one cycles, depending on transfer size and the parameter DW for the specific component. In general, this bit position of certain component is cleared to '0' upon system reset and is programmed during the system initialization process prior to begin access to it. However, the initial value of DW bit in BANK0 upon system reset should be determined by MSIZE pin causing the size should be definite while MCU fetches the first instruction from Flash device. Note that, dynamic changing this parameter will cause unexpected result.

0 16-bit device

1 8-bit device

EMI+0010h EMI Re-map Control Register EMI_REMAP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RM1	RM0
Type															R/W	R/W
Reset															BOOT	0

This register accomplishes the Memory Re-mapping Mechanism. Basically, it provides the kernel software program or system designer a capability of changing memory configuration dynamically. Three kinds of configuration are permitted.

RM[1:0] Re-mapping control for Boot Code, BANK0 and BANK1, refer to **Table 18**.

RM[1:0]	Address 00000000h (MB0)	Address 10000000h (MB1)
00	Boot Code	BANK1

01	BANK1	BANK0
10	BANK0	BANK1
11	BANK1	BANK0

Table 18 Memory Map Configuration

EMI+0014h EMI General Control Register EMI_GEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DS	PDE	KPE	PUE				EDA								
Type	R/W	R/W	R/W	R/W				R/W								
Reset	0	0	0	0				1								

This register is general control that can alter the behavior of all bank controllers according to specific features below.

DS Driving Strength of Output Buffers of EMI Interface

- **0** 4mA
- **2** 8mA

PDE Pull Down Control for ED[15:0]

- **0** Disable
- **1** Enable

KPE Keeper Control for ED[15:0]

- **0** Disable
- **1** Enable

PUE Pull Up Control for ED[15:0]

- **0** Disable
- **1** Enable

EDA ED[15:0] Activity

- **0** Drive ED Bus only on write access
- **1** Always drive ED Bus except for read access

EMI+0030h Code Cache and Code Prefetch Control Register PREFETCH_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MSB						PRE	CODE
Type									R/W						R/W	R/W
Reset									1						1	1

This register is used to control the functions of Code Cache and Code Prefetch. The Code Cache is a low latency memory that can store up to 10 most recently used instruction codes. While an instruction fetch hits the one in the code cache, not only the access time could be minimized, but also the singling to off chip ROM or Flash could be relieved. In addition, it can also store up to 10 prefetched instruction codes while Code Prefetch function is enabled. The Code Prefetch is a sophisticated controller that can predict and fetch the instruction codes in advance based on previous code fetching sequence. As the Code Prefetch always performs the fetch staffs during the period that the EMI interface is in IDLE state. The bandwidth to off chip memory could be fully utilized. On the other hand, if the instruction fetch hits the one of prefetched codes, the access time could be minimized and then enhance the overall system performance.

MSB Address Bit A[31:26] for Prefetchable Area

There bit positions determine the prefetchable and cacheable region in which the instruction codes could be cached or prefetched.

PRE Prefetch Function Enable

CODE Code Cache Enable

4 Microcontroller Peripherals

Microcontroller (MCU) Peripherals are devices that are under direct control of the Microcontroller. Most of them are attached to the Advanced Peripheral Bus (APB) of the MCU subsystem, thus shall serve as APB slaves. Each MCU peripheral has to be accessed as a memory-mapped I/O device, i.e., the MCU or the DMA bus master read or write specific peripheral by issuing memory-addressed transactions.

Following is the list of MCU peripherals:

- Pulse-Width Modulation Outputs
- Alerter
- SIM Interface
- Keypad Scanner
- LCD Interface
- General Purpose Inputs/Outputs
- Watchdog Timer
- Real Time Clock
- UART
- Baseband Serial Interface (BSI)
- Baseband Parallel Interface (BPI)
- Automatic Power Control (APC) Unit
- Automatic Frequency Control (AFC) Unit
- Auxiliary ADC unit
- General-Purpose Timers
- TDMA Timer
- MCU Coprocessors

Most of the above items will be mentioned in this chapter, while the others will be covered in other chapters according to their particular category of function.

4.1 Pulse-Width Modulation Outputs

4.1.1 General Description

Two generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duty cycle for LCD backlight or charging purpose. The duration of the PWM output signal is Low as long as the internal counter value is greater than or equals to the threshold value and the waveform is shown in **Figure 15**.

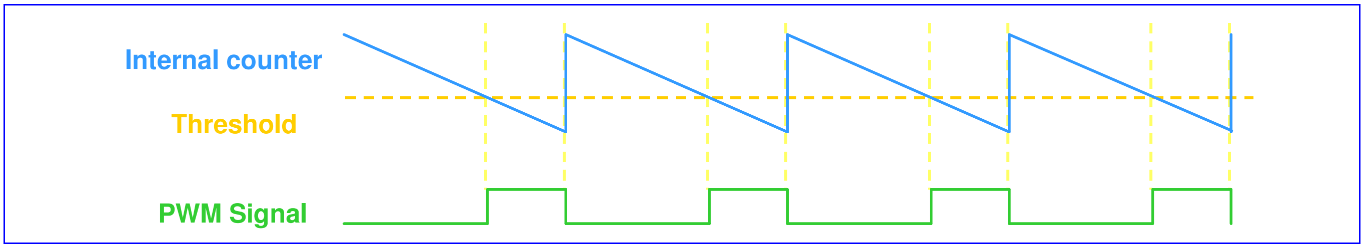

Figure 15 PWM waveform

The frequency and volume of PWM output signal are determined by these registers: PWM_COUNT, PWM_THRES, PWM_CON. POWERDOWN (pdn_pwm) signal is applied to power-down the PWM module. When PWM is deactivated (POWERDOWN=1), the output will in low state.

The output PWM frequency is determined by: $\frac{CLK}{(PWM_CON+1)\times 2\times (PWM_COUNT+1)}$ CLK = 13000000 when CLKSEL = 1, $CLK = 32000 when CLKSEL = 0$

The output PWM duty cycle is determined by: $\frac{PWM_THRES}{PWM_COUNT+1}$

Care should be taken that PWM_THRES should be less than the PWM_COUNT. If this condition is not satisfied, the output pulse of the PWM will be always in High state.

4.1.2 Register Definitions

PWM+0000h PWM1 Control register PWM1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLKSEL	CLK [1:0]	
Type														R/W	R/W	
Reset														0	0	

CLK Select PWM1 clock prescaler scale

00 CLK Hz

01 CLK/2 Hz

10 CLK/4 Hz

11 CLK/8 Hz

Note: When PWM1 module is disabled, its output should be keep in LOW state.

CLKSEL Select PWM1 clock

0 CLK=32K Hz

1 CLK=13M Hz

PWM+0004h PWM1 max counter value register PWM1_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_COUNT [12:0]												
Type				R/W												
Reset				1FFFh												

PWM1_COUNT PWM1 max counter value. It will be the initial value for the internal counter. If PWM1_COUNT is written when the internal counter is counting backwards, no matter which mode it is, there is no effect until the internal counter counts down to zero, i.e. a complete period.

PWM+0008h PWM1 Threshold Value register PWM1_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_THRES [12:0]												
Type				R/W												
Reset				0												

PWM1_THRES Threshold value. When the internal counter value is greater than or equals to PWM1_THRES, the PWM1 output signal will be "0"; when the internal counter is less than PWM1_THRES, the PWM1 output signal will be "1".

PWM+000Ch PWM2 Control register PWM2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLKSEL	CLK [1:0]	
Type														R/W	R/W	
Reset														0	0	

CLK Select PWM2 clock prescaler scale

- **00** CLK Hz
- **02** CLK/2 Hz
- **10** CLK/4 Hz
- **11** CLK/8 Hz

Note: When PWM2 module is disabled, its output should be keep in LOW state.

CLKSEL Select PWM2 clock

- **0** CLK=32K Hz
- **1** CLK=13M Hz

PWM+0010h PWM2 max counter value register PWM2_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM2_COUNT [12:0]												
Type				R/W												
Reset				1FFFh												

PWM2_COUNT PWM2 max counter value. It will be the initial value for the internal counter. If PWM2_COUNT is written when the internal counter is counting backwards, no matter which mode it is, there is no effect until the internal counter counts down to zero, i.e. a complete period.

PWM+0014h PWM2 Threshold Value register PWM2_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM2_THRES [12:0]												
Type				R/W												
Reset				0												

PWM2_THRES Threshold value. When the internal counter value is greater than or equals to PWM2_THRES, the PWM1 output signal will be "0"; when the internal counter is less than PWM2_THRES, the PWM2 output signal will be "1".

Figure 16 shows the PWM waveform with register value present.

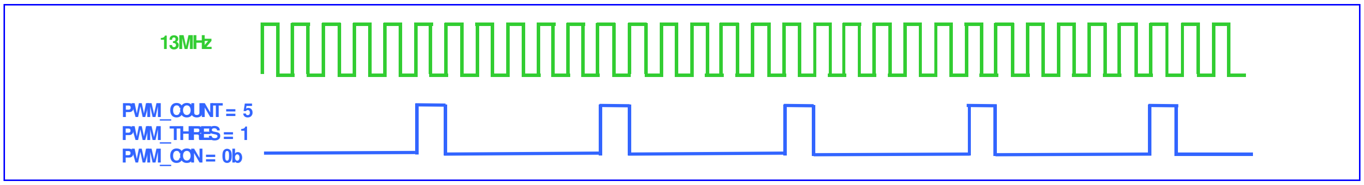

Figure 16 PWM waveform with register value present

4.2 Alerter

4.2.1 General Description

The output of Alerter has two sources: one is the enhanced pwm output signal, which is implemented embedded in Alerter module; the other is PDM signal from DSP domain directly. The enhanced pwm with three operation modes is implemented to generate a signal with programmable frequency and tone volume. The frequency and volume are determined by four registers: ALERTER_CNT1, ALERTER_THRES, ALERTER_CNT2 and ALERTER_CON. ALERTER_CNT1 and ALERTER_CNT2 are the initial counting values of internal counter1 and internal counter2 respectively. POWERDOWN signal is applied to power-down the Alerter module. When Alerter is deactivated (POWERDOWN=1), the output will be in low state.

With ALERTER_CON, the output source can be chosen from enhanced pwm or PDM. The waveform of the alerter from enhanced pwm source in different modes can be shown in **Figure 17**. In mode 1, the polarity of alerter output signal according to the relationship between internal counter1 and the programmed threshold will be inverted each time internal counter2 reaches zero. In mode2, each time the internal counter2 count backwards to zero the alerter output signal is normal pwm signal (i.e. signal is low as long as the internal counter1 value is greater than or equals to ALERTER_THRES, and it is high when the internal counter1 is less than ALERTER_THRES) or low state by turns. In mode3, the value of internal counter2 has no effect on output signal, i.e. the alerter output signal is low as long as the internal counter1 value is above the programmed threshold and is high the internal counter1 is less than ALERTER_THRES when no matter what value the internal counter2 is.

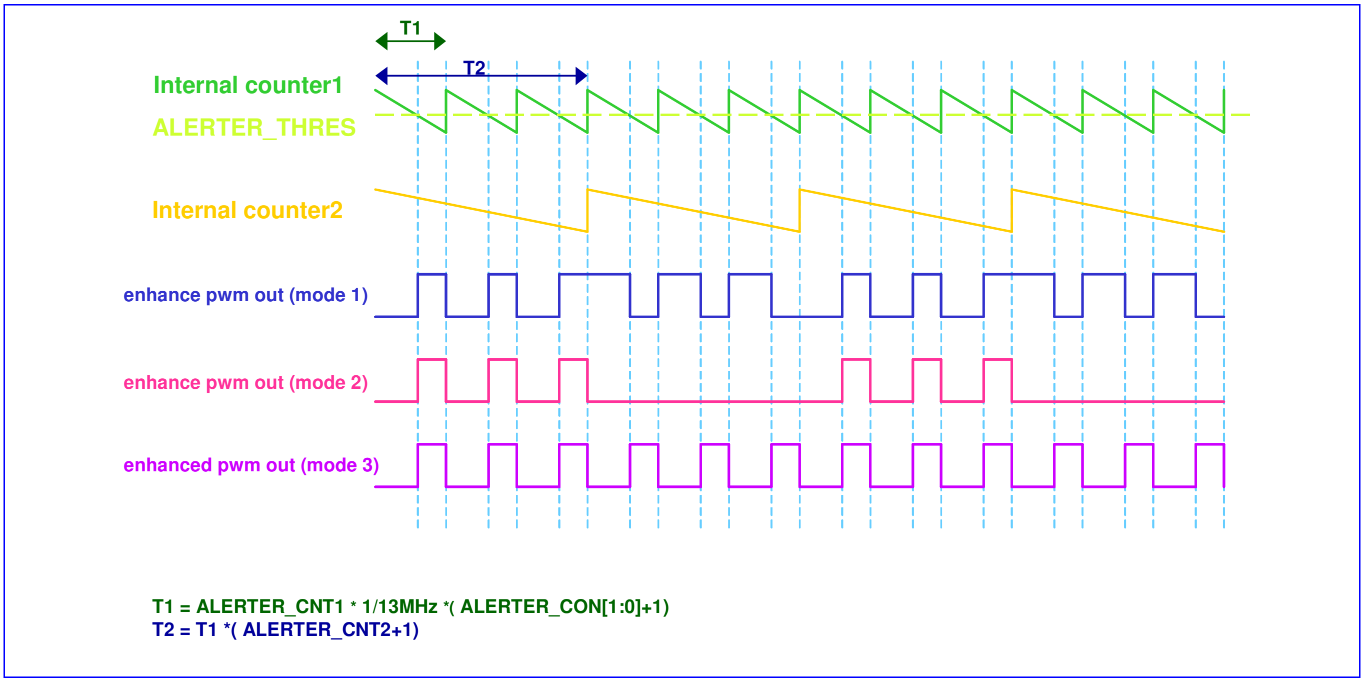

Figure 17 Alerter waveform

The output signal frequency is determined by:

$$\begin{cases} \dfrac{13000000}{2\times(ALERTER_CON[1:0]+1)\times(ALERTER_CNT1+1)\times(ALERTER_CNT2+1)} & \text{for mode 1 and mode 2} \\ \dfrac{13000000}{(ALERTER_CNT1+1)\times(ALERTER_CON[1:0])} & \text{for mode 3} \end{cases}$$

The volume of the output signal is determined by: $\dfrac{ALERTER_THRES}{ALERTER_CNT1+1}$

4.2.2 Register Definitions

ALTER+0000h Alerter counter1 value register — ALERTER_CNT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_CNT1 [15:0]															
Type	R/W															
Reset	FFFFh															

ALERTER_CNT1 Alerter max counter's value. ALERTER_CNT1 is the initial value of internal counter1. If ALERTER_CNT1 is written when the internal counter1 is counting backwards, no matter which mode it is, there is no effect until the internal counter1 counts down to zero, i.e. a complete period.

ALTER +0004h Alerter threshold value register — ALERTER_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_THRES [15:0]															

Type	R/W
Reset	0

ALERTER_THRES Threshold value. When the internal counter1 value is greater than or equals to ALERTER_THRES, the Alerter output signal will be low state; when the counter1 is less than ALERTER_THRES, the Alerter output signal will be high state.

ALTER +0008h Alerter counter2 value register ALERTER_CNT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALERTER_CNT2 [5:0]					
Type											R/W					
Reset											111111b					

AIERTER_CNT2 ALERTER_CNT2 is the initial value for internal counter2. The internal counter2 decreases by one everytime the internal counter1 count down to be zero. The polarity of alerter output signal which depends on the relationship between the internal counter1 and ALERTER_THRES will be inverted anytime when the internal counter2 counts down to zero. E.g. in the beginning, the output signal is low when the internal counter1 isn't less ALERTER_THRES and is high when the internal counter1 is less than ALERTER_THRES. But after the internal counter2 counts down to zero, the output signal will be high when the internal counter1 isn't less than ALERTER_THRES and will be low when the internal counter1 is less than ALERTER_THRES.

ALTER +000Ch Alerter control register ALERTER_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TYPE				MODE			CLK [1:0]	
Type								R/W				R/W			R/W	
Reset								0				0			0	

CLK Select PWM Waveform clock

00 13M Hz

01 13/2M Hz

10 13/4M Hz

11 13/8M Hz

MODE Select Alerter mode

00 Mode 1 selected

01 Mode 2 selected

10 Mode 3 selected

TYPE Select the ALERTER output source from PWM or PDM

0 Output generated from PWM path

1 Output generated from PDM path

Note: When alerter module is power down, its output should be kept in low state.

Figure 18 shows the Alerter waveform with register value present.

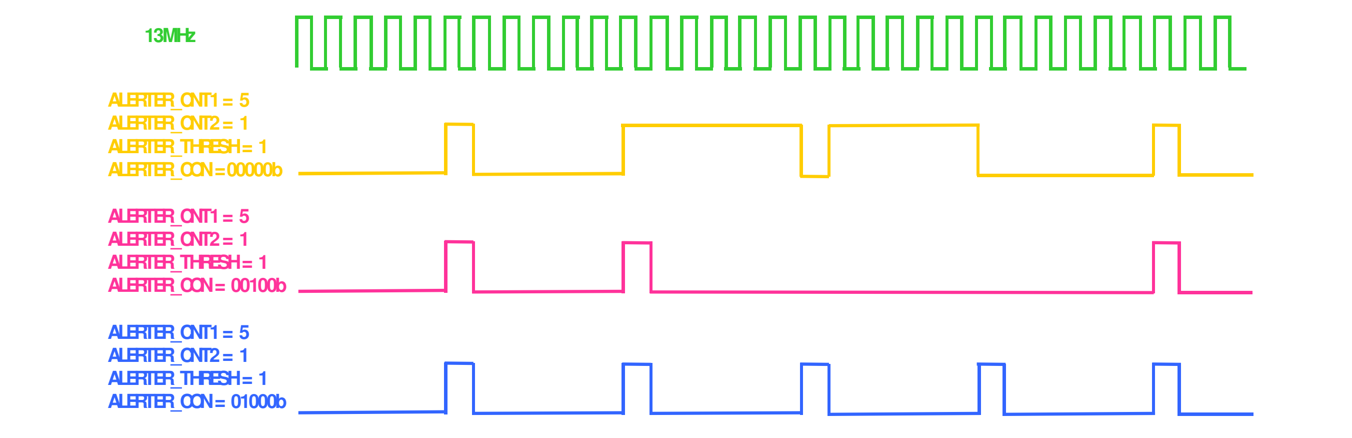

Figure 18 Alerter output signal from enhanced pwm with register value present

4.3 SIM Interface

The MT6205B contains a dedicated smart card interface to allow the MCU access to the SIM card. It can operate via 5 terminals, using SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA.

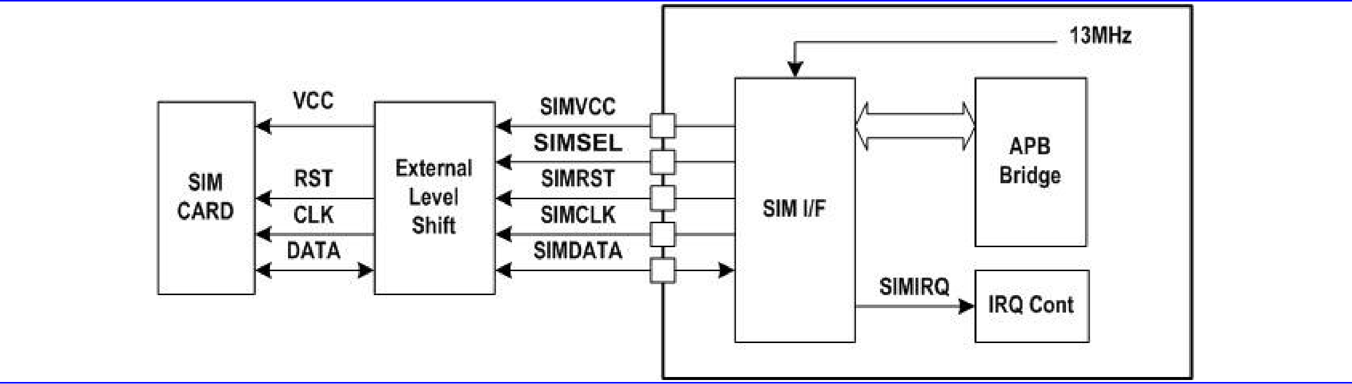

Figure 19 SIM Interface Block Diagram

The SIMVCC is used to control the external voltage supply to the SIM card and SIMSEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose.

Basically, the SIM interface acts as a half duplex asynchronous communication port and its data format is composed of ten consecutive bits: a start bit in state Low, eight information bits, and a tenth bit used for parity checking. The data format can be divided into two modes as follows:

<u>Direct Mode (ODD=SDIR=SINV=0)</u>

SB D0 D1 D2 D3 D4 D5 D6 D7 PB

SB: Start Bit (in state Low)

Dx: Data Byte (LSB is first and logic level ONE is High)

PB: Even Parity Check Bit

Indirect Mode (ODD=SDIR=SINV=1)

SB N7 N6 N5 N4 N3 N2 N1 N0 PB

SB: Start Bit (in state Low)

Nx: Data Byte (MSB is first and logic level ONE is Low)

PB: Odd Parity Check Bit

If the receiver gets a wrong parity bit, it will respond by pulling the SIMDATA Low to inform the transmitter and the transmitter will retransmit the character.

When the receiver is a SIM Card, the error response starts 0.5 bits after the PB and it may last for 1~2 bit periods.

When the receiver is the SIM interface, the error response starts 0.5 bits after the PB and lasts for 1.5 bit period.

When the SIM interface is the transmitter, it will take totally 14 bits guard period whether the error response appears. If the receiver shows the error response, the SIM interface will retransmit the previous character again else it will transmit the next character.

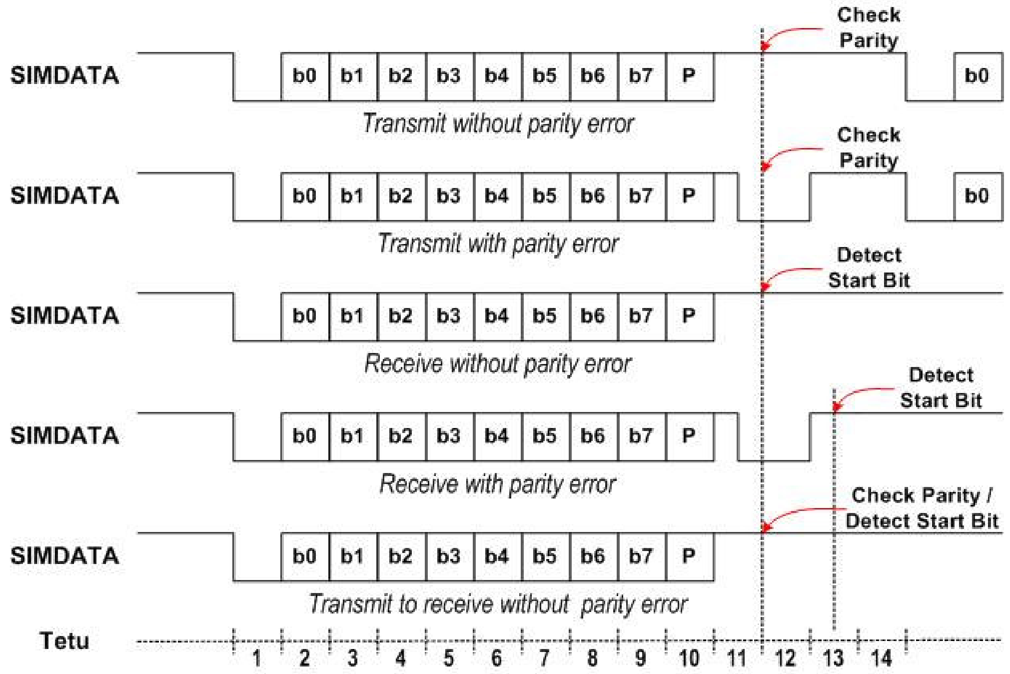

Figure 20 SIM Interface Timing Diagram

4.3.1 Register Definitions

SIM+0000h SIM module control register SIM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HALT	SIMON
Type															R/W	R/W
Reset															0	0

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SIMON SIM card power-up/power-down control

- **0** Initiate the card deactivation sequence
- **1** Initiate the card activation sequence

HALT Enable clock stop mode. Together with CLKPO in SIM_CNF register, it determines the polarity of the SIMCLK in this mode.

- **0** Enable the SIMCLK output.
- **1** Disable the SIMCLK output

SIM+0004h SIM module configuration register SIM_CNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						HFEN	T0EN	HALTEN	TOUT	SIMSEL	ODD	SDIR	SINV	CLKPOL	TXHSK	RXHSK
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

RXHSK SIM card reception error handshake control

- **0** Disable character receipt handshaking
- **1** Enable character receipt handshaking

TXHSK SIM card transmission error handshake control

- **0** Disable character transmission handshaking
- **1** Enable character transmission handshaking

CLKPOL SIMCLK polarity control in clock stop mode

- **0** Make SIMCLK stop in LOW level
- **1** Make SIMCLK stop in HIGH level

SINV Data Inverter.

- **0** Not invert the transmitted and received data
- **1** Invert the transmitted and received data

SDIR Data Transfer Direction

- **0** LSB is transmitted and received first
- **1** MSB is transmitted and received first

ODD Select odd or even parity

- **0** Even parity
- **1** Odd parity

SIMSEL SIM card supply voltage select

- **0** SIMSEL pin is set to LOW level
- **1** SIMSEL pin is set to HIGH level

TOUT SIM work waiting time counter control

- **0** Disable Time-Out counter
- **1** Enable Time-Out counter

HALTEN SIM card clock stop mode configuration

- **0** Clock stop mode is not provided by the SIM card
- **1** Clock stop mode is provided by the SIM card

T0EN T=0 protocol controller control

- **0** Disable T=0 protocol controller
- **1** Enable T=0 protocol controller

HFEN Hardware flow control

0 Disable hardware flow control

1 Enable hardware flow control

SIM +0008h SIM Baud Rate Register SIM_BRR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BAUD[1:0]		SIMCLK[1:0]	
Type													R/W		R/W	
Reset													00		01	

SIMCLK Set SIMCLK frequency

00 13/2 MHz

01 13/4 MHz

10 13/8 MHz

11 13/12 MHz

BAUD Determines the baud rate as a division of SIMCLK

00 SIMCLK/372

01 SIMCLK/64

10 SIMCLK/32

11 Reserved

SIM +000Ch SIM interrupt enable register SIM_IRQEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								0	0	0	0	0	0	0	0	0

For all these bits

0 Interrupt is disabled

1 Interrupt is enabled

SIM +0010h SIM module status register SIM_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type								R/C	R/C	R/C	R/C	R/C	R/C	R/C	R	R
Reset								—	—	—	—	—	—	—	—	—

TXTIDE Transmit FIFO tide mark reached interrupt occurred

RXTIDE Receive FIFO tide mark reached interrupt occurred

OVRUN Transmit/Receive FIFO overrun interrupt occurred

TOUT Between character timeout interrupt occurred

TXERR Character transmission error interrupt occurred

ATRERR ATR start time-out interrupt occurred

SIMOFF Card deactivation complete interrupt occurred

T0END Data Transfer handled by T=0 Controller completed interrupt occurred

RXERR Character reception error interrupt occurred

SIM +0014h Data register used as Tx/Rx Data Register SIM_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA[7:0]							
Type									R/W							
Reset									—							

DATA Eight data digits. These correspond to the character being read or written

SIM +0018h Character to character timeout register SIM_TOUT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIMTOUT[15:0]															
Type	R/W															
Reset	983h															

SIMTOUT Maximum interval between the leading edge of two consecutive characters in 4 ETU unit

SIM +001Ch SIM retry limit register SIM_RETRY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TXRETRY								RXRETRY		
Type						R/W								R/W		
Reset						3h								3h		

RXRETRY Specify the max. numbers of receive retries that are allowed when parity error has occurred.

TXRETRY Specify the max. numbers of transmit retries that are allowed when parity error has occurred.

SIM +0020h SIM FIFO tide mark register SIM_TIDE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXTIDE[3:0]								RXTIDE[3:0]			
Type					R/W								R/W			
Reset					0h								0h			

RXTIDE Trigger point for RXTIDE interrupt

TXTIDE Trigger point for TXTIDE interrupt

SIM +0024h SIM FIFO count register SIM_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													COUNT[3:0]			
Type													R/W			
Reset													0h			

COUNT The number of characters in the SIM FIFO when read, and flushes when written.

SIM +0028h SIM activation time register SIM_ATIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIMATIME[15:0]															
Type	R/W															
Reset	AFC7h															

SIMATIME The register defines the duration, in SIM clock cycles, of the time taken for each of the three stages of the card activation process

SIM +002Ch SIM deactivation time register SIM_DTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SIMDTIME[11:0]											
Type					R/W											
Reset					3E7h											

SIMDTIME The register defines the duration, in 13MHz clock cycles, of the time taken for each of the three stages of the card deactivation sequence

SIM +0030h SIM command header register: INS SIM_INS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INSD	SIMINS[7:0]							
Type								R/W	R/W							
Reset								0h	0h							

SIMINS This field should be identical to the INS instruction code. When writing to this register, the T=0 controller will be activated and data transfer will be initiated.

INSD [Description for this register field]

0 T=0 controller receives data from the SIM card

1 T=0 controller sends data to the SIM card

SIM +0034h SIM command header register: P3 SIM_P3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIMP3[8:0]								
Type								R/W								
Reset								0h								

SIMP3 This field should be identical to the P3 instruction code. It should be written prior to the SIM_INS register. While the data transfer is going on, this field shows the no. of the remaining data to be sent or to be received

SIM +0038h SIM procedure byte register: SW1 SIM_SW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW1[7:0]							
Type									R							
Reset									0h							

SIMSW1 This field holds the last received procedure byte for debug purpose. When the T0END interrupt occurred, it keeps the SW1 procedure byte.

SIM +003Ch SIM procedure byte register: SW2 SIM_SW2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW2[7:0]							
Type									R							
Reset									0h							

SIMSW2 This field holds the SW2 procedure byte

4.3.2 SIM Card Insertion and Removal

The detection of physical connection to the SIM card and card removal is done by the external interrupt controller or by GPIO.

4.3.3 Card Activation and Deactivation

The card activation and deactivation sequence both are controlled by H/W. The MCU initiates the activation sequence by writing a "1" to bit 0 of the SIM_CON register, and then the interface performs the following activation sequence:

- Assert SIMRST LOW
- Set SIMVCC at HIGH level and SIMDATA in reception mode
- Enable SIMCLK clock
- De-assert SIMRST HIGH (required if it belongs to active low reset SIM card)

The final step in a typical card session is contact deactivation in order that the card is not electrically damaged. The deactivation sequence is initiated by writing a "0" to bit 0 of the SIM_CON register, and then the interface performs the following deactivation sequence:

- Assert SIMRST LOW
- Set SCIMCLK at LOW level
- Set SIMDATA at LOW level
- Set SIMVCC at LOW level

4.3.4 Answer to Reset Sequence

After card activation, a reset operation results in an answer from the card consisting of the initial character TS, followed by at most 32 characters. The initial character TS provides a bit synchronization sequence and defines the conventions to interpret data bytes in all subsequent characters.

On reception of the first character, TS, MCU should read this character, establish the respective required convention and reprogram the related registers. These processes should be completed prior to the completion of reception of the next character. And then, the remainder of the ATR sequence is received, read via the SIM_DATA in the selected convention and interpreted by the S/W.

The timing requirement and procedures for ATR sequence are handled by H/W and shall meet the requirement of ISO 7816-3 as shown in **Figure 21**.

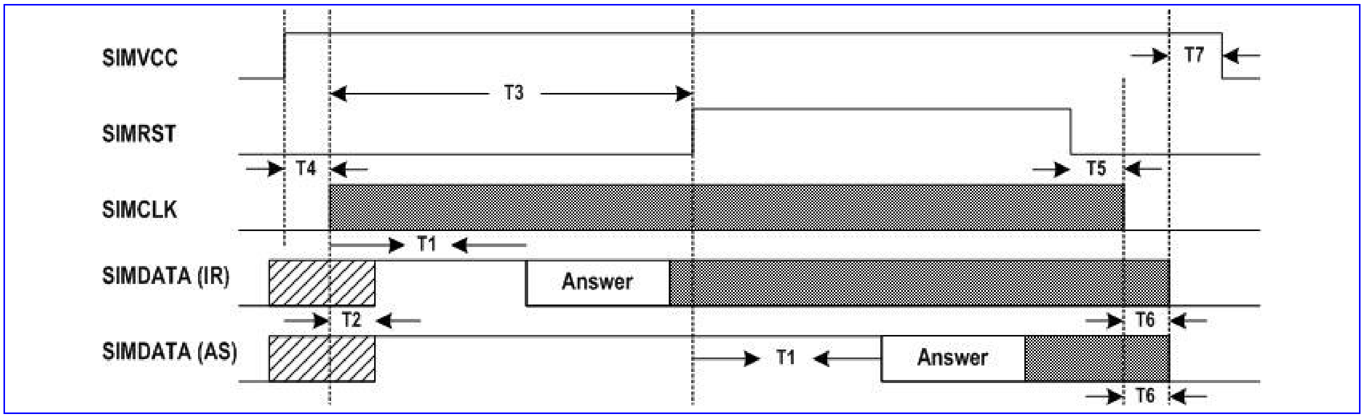

Figure 21 Answer to Reset Sequence

Time	Value	Comment
T1	> 400 SIMCLK	SIMCLK start to ATR appear
T2	< 200 SIMCLK	SIMCLK start to SIMDATA in reception mode
T3	> 40000 SIMCLK	SIMCLK start to SIMRST High
T4	—	SIMVCC High to SIMCLK start
T5	—	SIMRST Low to SIMCLK stop
T6	—	SIMCLK stop to SIMDATA Low
T7	—	SIMDATA Low to SIMVCC Low

Table 19 Answer to Reset Sequence Time-Out Condition

4.3.5 SIM Data Transfer

Two transfer modes are provided, either in software controlled byte by byte fashion or in a block fashion using T=0 controller and DMA controller. In both modes, the time-out counter could be enabled to monitor the elapsed time between two consecutive bytes.

4.3.5.1 Byte Transfer Mode

This mode is used during ATR and PPS procedure. In this mode, the SIM interface only ensures error free character transmission and reception.

Receiving Character

Upon detection of the start-bit sent by SIM card, the interface transforms into reception mode and the following bits are shifted into an internal register. If no parity error is detected or character-receive handshaking is disabled, the received-character is written into the SIM FIFO and the SIM_CNT register is increased by one. Otherwise, the SIMDATA line is held low at 0.5 etu after detecting the parity error for 1.5 etus, and the character is re-received. If a character fails to be received correctly for the RXRETRY times, the receive-handshaking is aborted and the last-received character is written into the SIM FIFO, the SIM_CNT is increased by one and the RXERR interrupt is generated

When the number of characters held in the receive FIFO exceeds the level defined in the SIM_TIDE register, a RXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_CNT register and writing to this register will flush the SIM FIFO.

Sending Character

Characters that are to be sent to the card are first written into the SIM FIFO and then automatically transmitted to the card at timed intervals. If character-transmit handshaking is enabled, the SIMDATA line is sampled at 1 etu after the parity bit. If the card indicates that it did not receive the character correctly, the character is retransmitted a maximum of TXRETRY times before a TXERR interrupt is generated and the transmission is aborted. Otherwise, the succeeding byte in the SIM FIFO is transmitted.

If a character fails to be transmitted and a TXERR interrupt is generated, the interface needs to be reset by flushing the SIM FIFO before any subsequent transmit or receive operation.

When the number of characters held in the SIM FIFO falls below the level defined in the SIM_TIDE register, a TXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_CNT register and writing to this register will flush the SIM FIFO.

4.3.5.2 Block Transfer Mode

Basically, the SIM interface is designed to work in conjunction with the T=0 protocol controller and the DMA controller during non-ATR and non-PPS phase, though it is still possible for software to service the data transfer manually like in byte transfer mode if necessary and thus the T=0 protocol should be controlled by software.

The T=0 controller is accessed via four registers representing the instruction header bytes INS and P3, and the procedure bytes SW1 and SW2. These registers are:

SIM_INS, SIM_P3

SIM_SW1, SIM_SW2

During characters transfer, SIM_P3 holds the number of characters to be sent or to be received and SIM_SW1 holds the last received procedure byte including NULL, ACK, NACK and SW1 for debug purpose.

Data Receive Instruction

Data Receive Instructions receive data from the SIM card. It is instantiated as the following procedure.

```
1. Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CNF register
2. Program the SIM_TIDE register to 0x0000 (TXTIDE = 0, RXTIDE = 0)
3. Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
4. Write CLA, INS, P1, P2 and P3 into SIM FIFO
5. Program the DMA controller :
   DMAn_MSBSRC and DMAn_LSBSRC : address of SIM_DATA register
   DMAn_MSBDST and DMAn_LSBDST : memory address reserved to store the received characters
   DMAn_COUNT : identical to P3 or 256 (if P3 == 0)
   DMAn_CON : 0x0078
6. Write P3 into SIM_P3 register and then INS into SIM_INS register (Data Transfer is initiated
   now)
7. Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CNF register
8. Start the DMA controller by writing 0x8000 into the DMAn_START register to
```

Upon completion of the Data Receive Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CNF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

Data Send Instruction

Data Send Instructions send data to the SIM card. It is instantiated as the following procedure.

```
1. Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CNF register
2. Program the SIM_TIDE register to 0x0100 (TXTIDE = 1, RXTIDE = 0)
3. Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
4. Write CLA, INS, P1, P2 and P3 into SIM FIFO
5. Program the DMA controller :
   DMAn_MSBSRC and DMAn_LSBSRC : memory address reserved to store the transmitted characters
   DMAn_MSBDST and DMAn_LSBDST : address of SIM_DATA register
   DMAn_COUNT : identical to P3
   DMAn_CON : 0x0074
```

```
6. Write P3 into SIM_P3 register and then (0x0100 | INS) into SIM_INS register (Data Transfer
   is initiated now)
7. Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CNF register
8. Start the DMA controller by writing 0x8000 into the DMAn_START register
```

Upon completion of the Data Send Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CNF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

4.4 Keypad Scanner

4.4.1 General Description

The keypad can be divided into two parts: one is the keypad interface including 5 columns and 5 rows; the other is the key detection block which provides key pressed, key released and de-bounce mechanism. Each time key pressed or key released, i.e. something different in the 5 x 5 matrix, the key detection block will sense it, and it will start to recognize if it's a key pressed or key released event. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key(s) pressed directly in KP_HI_KEY and KP_LOW_KEY registers. To ensure that the key pressed information won't be missed, the status register in keypad won't be read clear by APB bus read command. The status register only changes by the key-pressed detection FSM. This keypad can detect one or two key-pressed simultaneously with any combination. **Figure 22** shows one key pressed condition. **Figure 23**(a) and **Figure 23**(b) indicate two keys pressed cases. Since the key press detection depends on the high or low level of the external keypad interface, if keys are pressed at the same time and these exists one key is on the same column and the same row with the other keys, there will get a redundant key; e.g. there are three keys, key1 = (x1, y1), key2 = (x2, y2), key3 = (x1, y2), key4 = (x2, y1) will be detected, but key4 is a redundant one. Hence, the keypad can detect one or two keys pressed simultaneously at any combination. Due to the keypad interface, more than two keys pressed simultaneously with some specific pattern will get the wrong information. Without the specific pattern, the keypad-scanning block can detect 8 keys at the same time and it's shown as **Figure 24**.

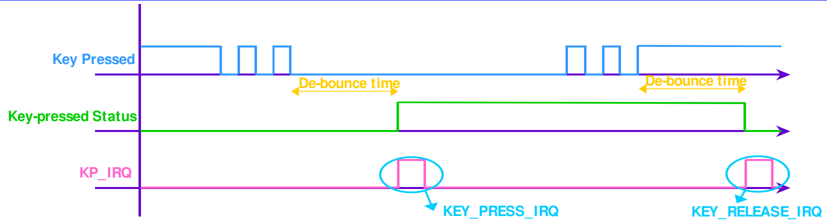

Figure 22 One key pressed with de-bounce mechanism denoted

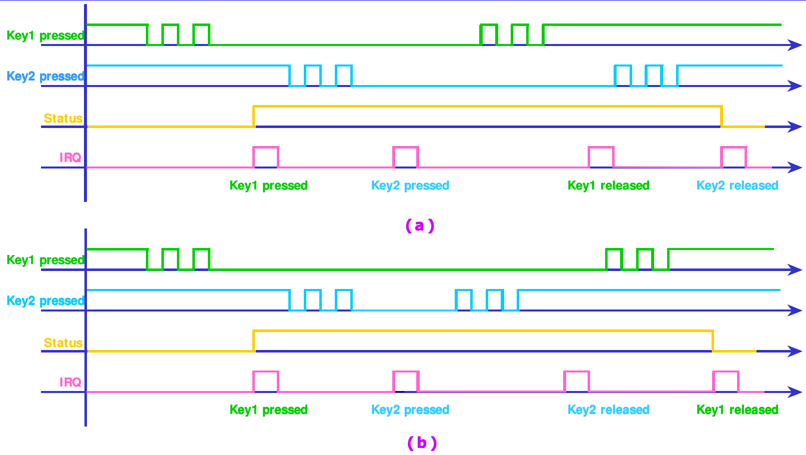

Figure 23 (a) Two keys pressed, case 1 **(b)** Two keys pressed, case 2

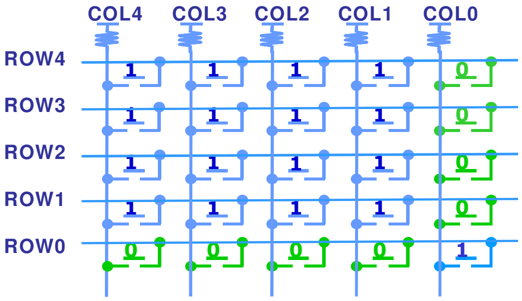

Figure 24 8 keys are detected at the same time

4.4.2 Register Definitions

KP +0000h Keypad status KP_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																R
Reset																0

STA This register indicates the keypad status, and it won’t be cleared by read.

0 No key pressed

1 Key pressed

KP +0004h Keypad scanning output, the lower 16 keys KP_LOW_KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYS [15:0]															
Type	R															
Reset	FFFFh															

KP +0008h Keypad scanning output, the higher 9 keys KP_HI_KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								KEYS [24:16]								
Type								R								

Reset								1FFh

These two registers list the status of 25 keys on the keypad. When the MCU receives the KEYPAD IRQ, both two registers must be read. If any key is pressed, the relative bit will be set to 0.

KEYS Status list of the 25 keys.

KP +0000Ch De-bounce period setting KP_DEBOUNCE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE [13:0]													
Type			R/W													
Reset			400h													

This register defines the waiting period before key press or release events are considering stale.

DEBOUNCE De-bounce time = KP_DEBOUNCE/32 ms

4.5 LCD Interface

A specific LCD DMA controller is implemented to allow MCU to access the external parallel or serial LCD module and to improve the data throughput for color LCD applications.

For parallel LCD modules, this special DMA controller reuses the external memory interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD module. Provided the external SRAM is the display data source, a special simultaneous read/write mode is provided to speed up the data transfer again.

For serial LCD modules, this interface performs parallel to serial conversion and both 8- and 9- bit serial interface is supported. The 8-bit serial interface uses four pins – LCD_CS#, LCD_DATA, LCD_DATA and LCD_A0 – to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins – LCD_CS#, LCD_DATA and LCD_CLK – for the same purpose. Data read is not available with the serial interface and data entered must be 8 bits.

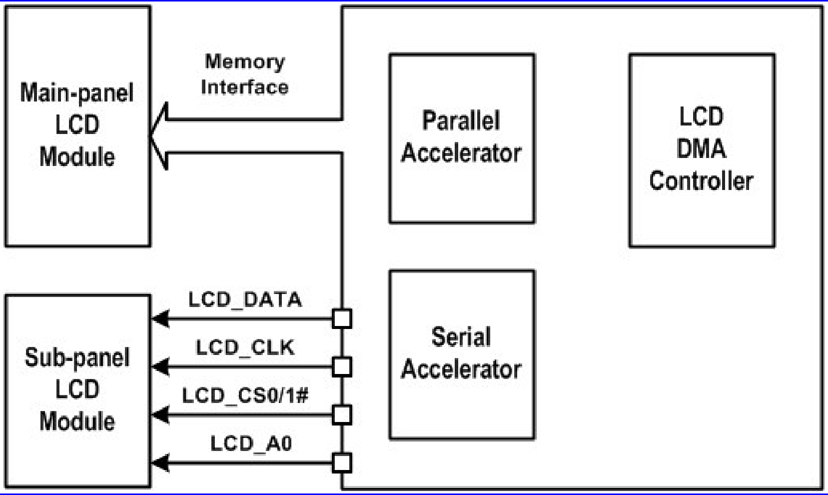

Figure 25 LCD Interface Block Diagram

Figure 26 shows the timing diagram of this serial interface. When the block is idle, LCD_CLK is forced LOW and LCD_CS# is forced HIGH. Once the data register contains data and the interface is enabled, LCD_CS# is pulled LOW and remain LOW for the duration of the transmission.

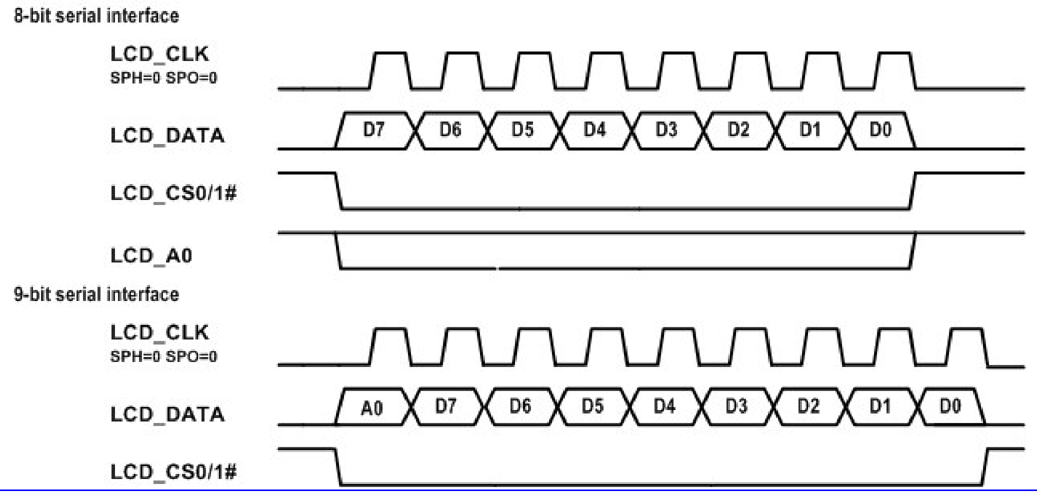

Figure 26 LCD Interface Transfer Timing Diagram

4.5.1 Register Definitions

LCD +0000h Parallel/Serial LCD Interface Global Status Register LCD_GSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SRUN	PRUN
Type															R/W	R/W
Reset															0	0

PRUN Parallel display interface running indication

SRUN Serial display interface running indication

LCD +0004h Parallel/Serial LCD Interface Interrupt Enable Register LCD_INTEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SOVR	PCPL
Type															R/W	R/W
Reset															0	0

PCPL Parallel display interface data transfer complete interrupt

SOVR Serial display interface data register overrun interrupt

LCD +0008h Parallel/Serial LCD Interface Interrupt Status Register LCD_INTSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SOVR	PCPL
Type															R/W	R/W
Reset															0	0

PCPL Parallel display interface data transfer complete interrupt

SOVR Serial display interface data register overrun interrupt

LCD +0010h Parallel LCD Interface Control Register LCD_PCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DINC	ACC							GRAD	
Type							R/W	R/W							R/W	
Reset							0	0							1	

GRAD Type of the LCD module coupled with parallel display interface

- **00** B/W Display or 256 Color Display
- **01** 4096 Color Display
- **10** Reserved
- **11** Reserved

ACC Enable Simultaneously Read/Write Operation

DINC Enable Destination Address Increasing

LCD +0014h Parallel LCD Interface Refresh Rate Register LCD_REFR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					REF											
Type					R/W											
Reset					63											

REF Data transfer period in 13MHz unit

LCD +0018h Parallel LCD Interface Refresh Start Register LCD_START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	START															
Type	R/W															
Reset	0															

START Start control of display interface DMA accelerator

LCD +001Ch Parallel LCD MSB Source Address Register LCD_MSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_SRC[31:16]															
Type	R/W															
Reset	0															

LCD +0020h Parallel LCD LSB Source Address Register LCD _LSBSRC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_SRC[15:0]															
Type	R/W															
Reset	000															

DISP_SRC Display Source Data Address

LCD +0024h Parallel LCD MSB Destination Address Register LCD _MSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DST[31:16]															
Type	R/w															
Reset	0															

LCD +0028h Parallel LCD LSB Destination Address Register LCD _LSBDST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DST[15:0]															
Type	R/W															
Reset	0															

DISP_DST Display Destination Data Address

LCD +002Ch Parallel LCD Module Page Area LCD _PASET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DISP_PAGE									
Type							R/W									
Reset							0									

DISP_PAGE Display Area Page Size

LCD +0030h Parallel LCD Module Column Area LCD _CASET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DISP_COL									
Type							R/W									
Reset							0									

DISP_COL Display Area Column Size

LCD +0034h Parallel LCD Module Column Hop Size LCD _CHOP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DISP_CHOP									
Type							R/W									
Reset							0									

DISP_CHOP Upon completing each page update, this offset value will be added to the current Display Source Address

LCD +0050h Serial LCD Interface Control Register LCD _SCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CS1PO	CS0PO				8/9	SCR		SPH	SPO
Type							R/W	R/W				R/W	R/W		R/W	R/W
Reset							0	0				0	00		0	0

SPO Clock Polarity Control
SPH Clock Phase Control
SCR Clock Rate Control
8/9 8-bit or 9-bit Interface Selection
CS0PO Chip Select 0 Polarity Control
CS1PO Chip Select 1 Polarity Control

LCD +0054h Serial LCD Interface Buffer Empty Status Register LCD _SSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EMP1	EMP0
Type															R/W	R/W

EMP0 Device 0 Data Register Empty Indication

EMP1 Device 1 Data Register Empty Indication

LCD +0060/64h Serial LCD Interface Data Register for Device 0 LCD _DATA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_DATA[7:0]							
Type									W							
Reset									—							

DISP_DATA Data Register for Device 0

LCD +0068/6Ch Serial LCD Interface Data Register for Device 1 LCD _DATA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_DATA[7:0]							
Type									W							
Reset									—							

DISP_DATA Data Register for Device 1

4.6 General Purpose Inputs/Outputs

MT-6205B offers 22 general-purpose I/O pins and 3 general-purpose output pins. By setting the control registers, MCU software can control the direction, the output value and read the input values on these pins. Besides, these GPIOs and GPOs are multiplexed with other functionalities to reduce the pin count.

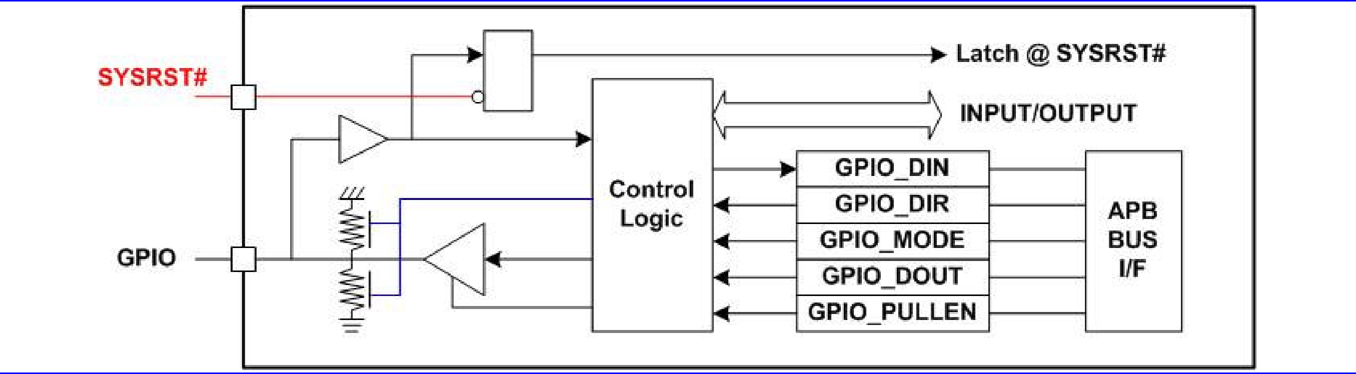

Figure 27 GPIO Block Diagram

GPIOs at RESET

At hardware reset (SYSRST#), GPIOs are all configured as inputs and the following alternative uses of GPIO pins are made:

- GPIO[0] is used as the **BOOT** input for memory map indication [1]
- GPIO[1] is used as the **MSIZE** input for boot rom size indication

[1] For detailed BOOT and MSIZE configuration, please see in Micro-Controller Unit System section

These GPIOs are used to latch the inputs at reset to memorize the wanted configuration to make sure that the system restarts or boots in the right mode.

Multiplexing of Signals on GPIO

The GPIO pins can be multiplexed with other signals.

- DAICLK, DAIPCMIN, DAIPCMOUT, DAIRST: digital audio interface for FTA
- BPI_BUS4, BPI_BUS5, BPI_BUS6, BPI_BUS7: radio hard-wire control
- BSI_CS1: additional chip select signal for radio 3-wire interface
- LCD_CS0#, LCD_CS1#, LCD_DATA, LCD_CLK, LCD_A0: serial display interface
- PWM: pulse width modulation signal
- UDSR1, UDTR1: hardware flow control signals for UART1
- URXD2, UTXD2, UCTS2, URTS2: data and flow control signals for UART2
- UREF_CK: UART1 external reference clock for high speed download
- External nIRQ: External interrupt for battery remove indication

Multiplexed of Signals on GPO

- EA22: external memory interface address pin 22
- SRCLKENA, SRCLKENAN: power on signal of the external VCXO LDO
- XLCDE: address signal for 68K parallel LCD interface

4.6.1 Register Definitions

GPIO+0000h GPIO direction control register 1 GPIO_DIR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO*n* GPIO direction control

0 GPIOs are configured as input

1 GPIOs are configured as output

GPIO +0004h GPIO direction control register 2 GPIO_DIR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

GPIO*n* GPIO direction control

0 GPIOs are configured as input

1 GPIOs are configured as output

GPIO +0008h GPIO pull-up/pull-down enable register 1 GPIO_PULLEN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GPIO*n* GPIO pull-up/pull-down control

- **0** Pull-up/pull-down of GPIO are disabled
- **1** Pull-up/pull-down of GPIO are enabled

GPIO +000Ch GPIO pull-up/pull-down enable register 2 GPIO_PULLEN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											1	1	1	1	1	1

GPIO*n* GPIO pull-up/pull-down control

- **0** Pull-up/pull-down of GPIO are disabled
- **1** Pull-up/pull-down of GPIO are enabled

GPIO +0010h GPIO data output register 1 GPIO_DOUT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +0014h GPIO data output register 2 GPIO_DOUT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

GPIO +0018h GPIO data Input register 1 GPIO_DIN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO +001Ch GPIO data Input register 2 GPIO_DIN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type											R	R	R	R	R	R
Reset											X	X	X	X	X	X

GPIO +0020h GPO data output register GPO_DOUT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GPO2	GPO1	GPO0
Type														R/W	R/W	R/W
Reset														0	0	0

GPIO +0024h GPIO mode control register 1 GPIO_MODE1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO7_M		GPIO6_M		GPIO5_M		GPIO4_M		GPIO3_M		GPIO2_M		GPIO1_M		GPIO0_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		00		00		00		00		00		00		00	

GPIO0_M GPIO mode selection

- **00** Configured as GPIO function
- **01** DAICLK
- **10** Reserved
- **11** Reserved

GPIO1_M GPIO mode selection

- **00** Configured as GPIO function
- **01** DAIPCMOUT
- **10** Reserved
- **11** Reserved

GPIO2_M GPIO mode selection

- **00** Configured as GPIO function
- **01** DAIPCMIN
- **10** Reserved
- **11** Reserved

GPIO3_M GPIO mode selection

- **00** Configured as GPIO function
- **01** DAIRST
- **10** Reserved
- **11** Reserved

GPIO4_M GPO mode selection

- **00** Configured as GPIO function
- **01** BPI_BUS4
- **10** Reserved
- **11** Reserved

GPIO5_M GPIO mode selection

00 Configured as GPIO function
01 BPI_BUS5
10 Reserved
11 Reserved
GPIO6_M GPIO mode selection
00 Configured as GPIO function
01 BPI_BUS6
10 Reserved
11 Reserved
GPIO7_M GPIO mode selection
00 Configured as GPIO function
01 BPI_BUS7
10 BSI_CS1
11 Reserved

GPIO +0028h GPIO mode control register 2 GPIO_MODE2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_M		GPIO14_M		GPIO13_M		GPIO12_M		GPIO11_M		GPIO10_M		GPIO9_M		GPIO8_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		00		00		00		00		00		00		00	

GPIO8_M GPIO mode selection
00 Configured as GPIO function
01 LCD_DATA
10 Reserved
11 Reserved
GPIO9_M GPIO mode selection
00 Configured as GPIO function
01 LCD_A0
10 Reserved
11 Reserved
GPIO10_M GPIO mode selection
00 Configured as GPIO function
01 LCD_CLK
10 Reserved
11 Reserved
GPIO11_M GPIO mode selection
00 Configured as GPIO function
01 LCD_CS0#
10 Reserved
11 Reserved
GPIO12_M GPIO mode selection
00 Configured as GPIO function
01 LCD_CS1#
10 Reserved

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11 Reserved

GPIO13_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 Reserved

GPIO14_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 Reserved

GPIO15_M GPIO mode selection

00 Configured as GPIO function

01 Reserved

10 Reserved

11 Reserved

GPIO +002Ch GPIO mode control register 3 GPIO_MODE3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO21_M		GPIO20_M		GPIO19_M		GPIO18_M		GPIO17_M		GPIO16_M	
Type					R/W		R/W		R/W		R/W		R/W		R/W	
Reset					00		00		00		00		00		00	

GPIO16_M GPIO mode selection

00 Configured as GPIO function

01 PWM

10 Reserved

11 Reserved

GPIO17_M GPIO mode selection

00 Configured as GPIO function

01 UCTS2

10 UDSR1

11 Reserved

GPIO18_M GPIO mode selection

00 Configured as GPIO function

01 URTS2

10 UDTR1

11 Reserved

GPIO19_M GPIO mode selection

00 Configured as GPIO function

01 URXD2

10 Reserved

11 Reserved

GPIO20_M GPIO mode selection

00 Configured as GPIO function

01 UTXD2
10 Reserved
11 Reserved

GPIO21_M GPIO mode selection
00 Configured as GPIO function
01 UREF_CK
10 External nIRQ
11 Reserved

GPIO +0030h GPIO mode control register 4 GPIO_MODE4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									GPO3_M		GPO2_M		GPO1_M		GPO0_M	
Type									R/W		R/W		R/W		R/W	
Reset									01		01		01		10	

GPO0_M GPO mode selection
00 Configured as GPO function
01 XLCDE
10 EA22
11 Reserved

GPO1_M GPO mode selection
00 Configured as GPO function
01 SRCLKENAN
10 Reserved
11 Reserved

GPO2_M GPO mode selection
00 Configured as GPO function
01 SRCLKENA
10 Reserved
11 Reserved

GPO3_M GPO mode selection
00 Configured as GPO function
01 Alerter
10 Reserved
11 Reserved

4.7 General Purpose Timer

4.7.1 General Description

Two general-purpose timers, that are 16 bit long and runs independently with the same clock source are provided. Each timer can operate in two modes: one-shot mode and auto-repeat mode. In one-shot mode, when the timer counts down and reaches zero, it is halted. In auto-repeat mode, as the timer reaches zero, it will simply reset and continue counting backward until the disable signal is set to be one. If the initial counting value (i.e. GPTIMER1_DAT for GPT1 or GPTIMER_DAT2 for GPT2) is written when the timer is running, no matter which mode it is, there is no effect until the

next time the timer is restarted. Hence, be sure to set the destined values for GPTIMER_DAT and the GPTIMER_PRESCALER registers before enable the gptimer.

4.7.2 Register Definitions

GPT +0000h GPT1 Control register GPTIMER1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

MODE This register controls GPT1 to count repeatedly or just one-shot

- **0** One-shot mode is selected
- **1** Auto-repeat mode is selected

EN This register controls GPT1 starts to count or disables it

- **0** GPT1 is disabled
- **1** GPT1 is enabled

GPT +0004h GPT1 Time-Out Interval register GPTIMER1_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT1 will count down from GPTIMER1_DAT. When GPT1 counts down to zero, interrupt of GPT1 will be generated.

GPT +0008h GPT2 Control register GPTIMER2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

MODE This register controls GPT2 to count repeatedly or just one-shot

- **0** One-shot mode is selected
- **1** Auto-repeat mode is selected

EN This register controls GPT2 starts to count or disables it

- **0** GPT2 is disabled
- **1** GPT2 is enabled

GPT +000Ch GPT2 Time-Out Interval register GPTIMER2_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT2 will count down from GPTIMER2_DAT. When GPT2 counts down to zero, interrupt of GPT2 will be generated.

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GPT +0010h GPT Status register GPTIMER_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT2	GPT1
Type															R/C	R/C
Reset															0	0

This register is for illustrating of the gptimer time out status. Each flag is set when the corresponding counter countdown finished, and can be cleared when the CPU reads the status register.

GPT +0014h GPT1 Prescaler register GPTIMER1_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the gptimer1 counting clock

- **000** 16K Hz
- **001** 8K Hz
- **010** 4K Hz
- **011** 2K Hz
- **100** 1K Hz
- **101** 500Hz
- **110** 250Hz
- **111** 125Hz

GPT +0018h GPT2 Prescaler register GPTIMER2_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the gptimer2 counting clock

- **000** 16K Hz
- **001** 8K Hz
- **010** 4K Hz
- **011** 2K Hz
- **100** 1K Hz
- **101** 500Hz
- **110** 250Hz
- **111** 125Hz

4.8 UART

4.8.1 General Description

The MT6205B houses two UARTs. Besides a full-functional UART, there is another simplified UART for displaying debugging messages. The UARTs provide full duplex serial communication channels between the MT6205B and external devices.

The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but there are some areas where there is no consensus.

In common with the M16550A, the UART supports word lengths from five to eight bits, an optional parity bit and one or two stop bits, and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, which are used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of 10 sources.

Note: The UART has been designed so that all internal operations are synchronized by the CLK signal. This results in minor timing differences between the UART and the industry standard 16550A device, which mean that the core is not clock for clock identical to the original device.

After a hardware reset, the UART is in M16C450 mode. It can then have its FIFOs enabled and enter M16550A mode. The UART then adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

The UART provides more powerful enhancements than the industry-standard 16550:

- Hardware flow control. This is a very useful feature when the ISR latency is hard to predict and control in the embedded applications. It relieves the MCU from having to fetch the received data within a fixed amount of time.
- Output of an IR-compatible electrical pulse with a width 3/16 of that of a regular bit period.

Note: In order to enable any of the enhancements, the Enhanced Mode bit, EFR[4], has to be set. If EFR[4] is not set, it is not possible to write to IER[7:5], FCR[5:4], ISR[5:4] and MCR[7:6]. This is to ensure that the UART is backward compatible for software that has been written for 16C450 and 16550A devices.

Figure 28 shows the block diagram of the 6205B UART device.

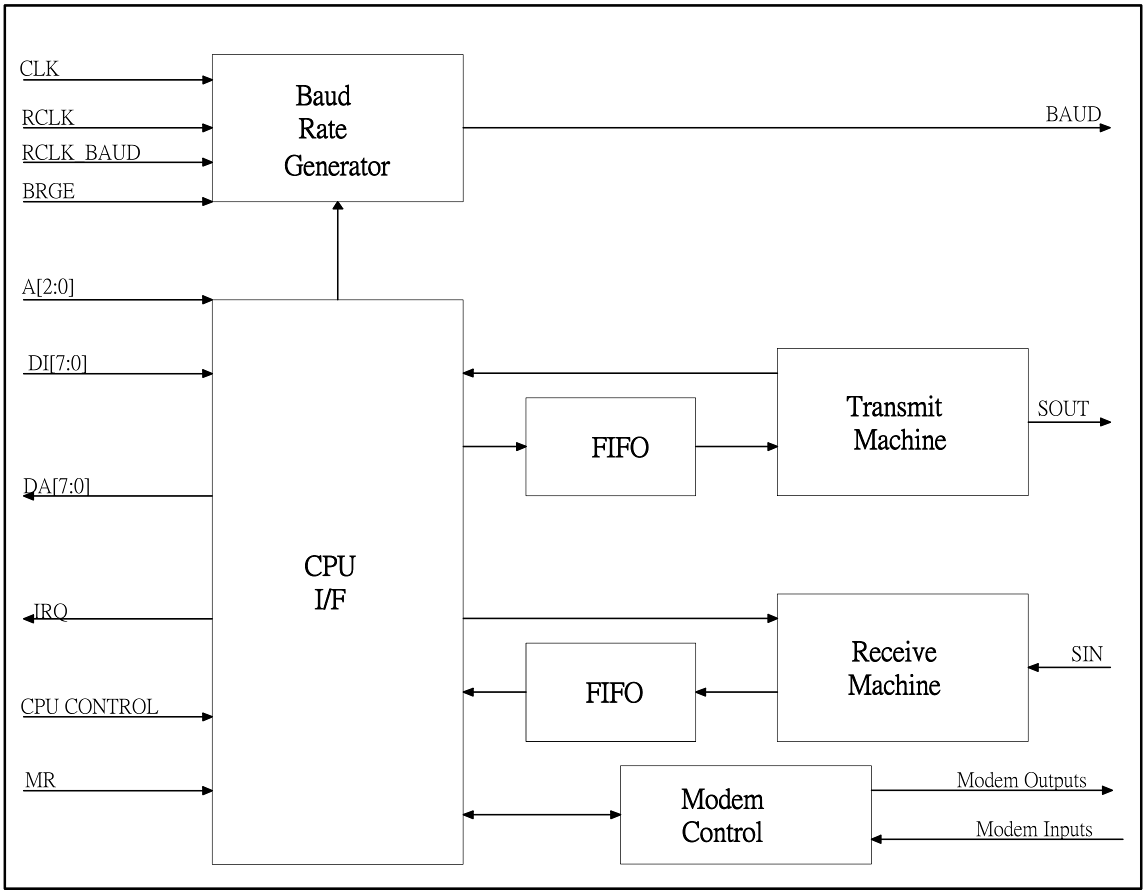

Figure 28 Block Diagram of UART

4.8.2 Register Definition

n = 1, 2 for uart1 and uart2 respectively.

UARTn+0000h RX Buffer Register UART_RBR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR[7:0]							
Type									R							

RBR RX Buffer Register. This is a read-only register. The received data can be read by accessing this register.

UARTn+0000h TX Holding Register UART_THR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR[7:0]							
Type									W							

THR TX Holding Register. This is a write-only register. The data to be transmitted is written to this register, and then sent to PC via serial communication.

UARTn+0004h Interrupt Enable Register UART_IER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI	X	EDSSI	ELSI	ETBEI	ERBFI
Type									R/W							
Reset									0							

IER By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled.

CTSI Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.
Note: This interrupt is only enabled when hardware flow control is enabled

- **0** Un-mask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
- **1** Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line.

RTSI Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.
Note: This interrupt is only enabled when hardware flow control is enabled

- **0** Un-mask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
- **1** Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line.

XOFFI Masks an interrupt that is generated when an XOFF character is received.
Note: This interrupt is only enabled when software flow control is enabled

- **0** Un-mask an interrupt that is generated when an XOFF character is received.
- **1** Mask an interrupt that is generated when an XOFF character is received.

EDSSI When set ("1"), an interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

- **0** No interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.
- **1** An interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

ELSI When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

- **0** No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
- **1** An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

ETBEI When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.

- **0** No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
- **1** An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level

ERBFI When set ("1"), an interrupt is generated if the RX Buffer contains data.

- **0** No interrupt is generated if the RX Buffer contains data.
- **1** An interrupt is generated if the RX Buffer contains data.

UARTn+0008h Interrupt Identification Register UART_IIR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID4	ID3	ID2	ID1	ID0	NINT
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

IIR Identify if there are pending interrupts.

The following table gives the IIR[5:0] codes associated with the possible interrupts:

IIR[5:0]	Priority Level	Interrupt	Source

00001	-	No interrupt pending	
000110	1	Line Status Interrupt	BI, FE, PE or OE set in LSR
000100	2	RX Data Received	RX Data received or RX Trigger Level reached.
001100	2	RX Data Timeout	Timeout on character in RX FIFO.
000010	3	TX Holding Register Empty	TX Holding Register empty or TX FIFO Trigger Level reached.
000000	4	Modem Status change	DDCD, TERI, DDSR or DCTS set in MSR
010000	5	Software Flow Control	XOFF Character received
100000	6	Hardware Flow Control	CTS or RTS Rising Edge

Table 20 IIR[5:0] codes associated with the possible interrupts

FIFOE Indicates if FIFOs are enabled.

0 FIFOs disabled.

1 FIFOs enabled.

UARTn+0008h FIFO Control Register UART_FCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1	RFTL0	TFTL1	TFTL0	DMA1	CLRT	CLRR	FIFOE
Type									W							

FCR FCR is used to control the trigger levels of the FIFOs, or flush the FIFOs.

FCR[7:6] RX FIFO trigger threshold.

00 1

01 4

10 8

11 14

FCR[5:4] TX FIFO trigger threshold.

00 1

01 4

10 8

11 14

DMA1 This bit determines the DMA mode which the TXRDY and RXRDY pins support. Note that this bit has no effect unless the FIFOE bit is set as well.

0 The device operates in DMA Mode 0.

1 The device operates in DMA Mode 1.

CLRT Clear Transmit FIFO. This bit is self-clearing.

0 Leave TX FIFO intact.

1 Clear all the bytes in the TX FIFO.

CLRR Clear Receive FIFO. This bit is self-clearing.

0 Leave RX FIFO intact.

1 Clear all the bytes in the RX FIFO.

FIFOE FIFO Enabled. This bit must be a 1 for any of the other bits in the registers to have any effect.

0 Disable both the RX and TX FIFOs.

1 Enable both the RX and TX FIFOs.

UARTn+000Ch Line Control Register UART_LCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1	WLS0
Type									R/W							
Reset									0	0	0	0	0	0	0	0

LCR Line Control Register. Determine characteristics of serial communication signals

DLAB Divisor Latch Access Bit.

0 The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4.

1 The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.

SB Set Break

0 No effect.

1 SOUT signal is forced into the "0" state.

SP Stick Parity

0 No effect.

1 The Parity bit is forced into a defined state, dependent upon state of EPS and PEN:
If EPS = "1" & PEN = "1", the Parity bit is set and checked = "0".
If EPS = "0" & PEN = "1", the Parity bit is set and checked = "1".

EPS Even Parity Select

0 When EPS="0", an odd number of ones is sent and checked.

1 When EPS="1", an even number of ones is sent and checked.

PEN Parity Enable

0 The Parity is neither transmitted nor checked.

1 The Parity is transmitted and checked.

STB Number of Stop Bits

0 One STOP bit is always added.

1 Two STOP bits are added after each character is sent, unless the character length is 5 when 1 STOP bit is added.

WLS1, 0 Word Length Select.

00 5 bits.

01 6 bits.

10 7 bits.

11 8 bits.

UARTn+0010h Modem Control Register UART_MCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF STATUS	IR ENABLE	X	LOOP	OUT2	OUT1	RTS	DTR
Type									R/W							
Reset									0	0	0	0	0	0	0	0

MCR Modem Control Register. Control interface signals of the UART.

XOFF Status This is a read-only bit.

- **0** When an XON character is received.
- **1** When an XOFF character is received.

IR Enable Enable IrDA modulation/demodulation.

- **0** Disable IrDA modulation/demodulation.
- **1** Enable IrDA modulation/demodulation.

LOOP Loop-back control bit.

- **0** No loop-back is enabled.
- **1** Loop-back mode is enabled.

OUT2 Control the state of the output NOUT2, even in loop mode.

- **0** NOUT2=”1”.
- **1** NOUT2=”0”.

OUT1 Control the state of the output NOUT1, even in loop mode.

- **0** NOUT1=”1”.
- **1** NOUT1=”0”.

RTS Control the state of the output NRTS, even in loop mode.

- **0** NRTS=”1”.
- **1** NRTS=”0”.

DTR Control the state of the output NDTR, even in loop mode.

- **0** NDTR=”1”.
- **1** NDTR=”0”.

UARTn+0014h Line Status Register UART_LSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									R/W							
Reset									0	1	1	0	0	0	0	0

LSR Line Status Register.

FIFOERR RX FIFO Error Indicator.

- **0** No PE, FE, BI set in the RX FIFO.
- **1** Set to 1 when there is at least one PE, FE or BI in the RX FIFO.

TEMT TX Holding Register (or TX FIFO) and the TX Shift Register are empty.

- **0** Empty conditions below are not met.
- **1** If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

THRE Indicate if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.

- **0** When at least one byte is written to the TX FIFO or the TX Shift Register.
- **1** Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled.)

BI Break Interrupt.

- **0** Reset by the CPU reading this register.
- **1** If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits).

If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.

FE Framing Error.

0 Reset by the CPU reading this register.

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.

PE Parity Error

0 Reset by the CPU reading this register.

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.

OE Overrun Error

0 Reset by the CPU reading this register.

1 If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents.

If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but it is not transferred to the FIFO.

DR Data Ready.

0 Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes.

1 Set by the RX Buffer becoming full or by a byte being transferred into the FIFO.

UARTn+0018h Modem Status Register — UART_MSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									Input	Input	Input	Input	0	0	0	0

Note: After reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing ‘0’ or set by writing ‘1’ to this register. D0-D3 can be written to.

MSR Modem Status Register.

DCD Data Carry Detect.

When Loop = "0", this is the complement of the NDCD input signal.

When Loop = "1", this is equal to the OUT2 bit in the Modem Control Register.

RI Ring Indicator.

When Loop = "0", this is the complement of the NRI input signal.

When Loop = "1", this is equal to the OUT1 bit in the Modem Control Register.

DSR Data Set Ready

When Loop = "0", this is the complement of the NDSR input signal.

When Loop = "1", this is equal to the DTR bit in the Modem Control Register.

CTS Clear To Send.

When Loop = "0", this is the complement of the NCTS input signal.

When Loop = "1", this is equal to the RTS bit in the Modem Control Register.

DDCD Delta Data Carry Detect.

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0 The state of DCD has not changed since the Modem Status Register was last read.

1 Set if the state of DCD has changed since the Modem Status Register was last read.

TERI Trailing Edge Ring Indicator

0 The NRI input does not change since this register was last read.

1 Set if the NRI input changes from “0” to “1” since this register was last read.

DDSR Delta Data Set Ready

0 Cleared if the state of DSR has not changed since this register was last read.

1 Set if the state of DSR has changed since this register was last read.

DCTS Delta Clear To Send

0 Cleared if the state of CTS has not changed since this register was last read.

1 Set if the state of CTS has changed since this register was last read.

UARTn+001Ch Scratch Register UART_SCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR[7:0]							
Type									R/W							

A general-purpose read/write register. After reset, its value is un-defined.

UARTn+0000h Divisor Latch (LS) UART_DLL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL[7:0]							
Type									R/W							
Reset									1							

UARTn+0004h Divisor Latch (MS) UART_DLM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL[7:0]							
Type									R/W							
Reset									0							

Note: DLL & DLM can only be updated if DLAB is set (“1”). Note too that division by 1 generates a BAUD signal that is constantly high.

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13 and 26MHz. The effective clock enable generated is 16 x the required baud rate.

BAUD	13 MHz	26 MHz
110	7386	14773
300	2708	5417
1200	677	1354
2400	338	677
4800	169	339
9600	85	169
19200	42	85
38400	21	42

57600	14	28
115200	7	14

Table 21 Divisor needed to generate a given baud rate

UARTn+0008h Enhanced Feature Register UART_EFR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO CTS	AUTO RTS	D5	ENAB LE-E	SW FLOW CONT [3:0]			
Type									R/W	R/W	R/W	R/W	R/W			
Reset									0	0	0	0	0			

*NOTE: Only when LCR=BFh

Auto CTS Enables hardware transmission flow control
- **0** Disabled.
- **1** Enabled.

Auto RTS Enables hardware reception flow control
- **0** Disabled.
- **1** Enabled.

Enable-E Enable enhancement features.
- **0** Disabled.
- **1** Enabled.

CONT[3:0] Software flow control bits.
- **00xx** No TX Flow Control
- **10xx** Transmit XON1/XOFF1 as flow control bytes
- **01xx** Transmit XON2/XOFF2 as flow control bytes
- **11xx** Transmit XON1 & XON2 and XOFF1 & XOFF2 as flow control words
- **xx00** No RX Flow Control
- **xx10** Receive XON1/XOFF1 as flow control bytes
- **xx01** Receive XON2/XOFF2 as flow control bytes
- **xx11** Receive XON1 & XON2 and XOFF1 & XOFF2 as flow control words

UARTn+0010h XON1 UART_XON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1 [7:0]							
Type									R/W							
Reset									0							

UARTn+0014h XON2 UART_XON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2 [7:0]							
Type									R/W							
Reset									0							

UARTn+0018h XOFF1 UART_XOFF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									XOFF1 [7:0]							
Type									R/W							
Reset									0							

UARTn+001Ch XOFF2 UART_XOFF2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2 [7:0]							
Type									R/W							
Reset									0							

*Note: XON1, XON2, XOFF1, XOFF2 are valid only when LCR=BFh.

UARTn +0020h RATE_STEP RATE_STEP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RATE_STEP [1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

RATE_STEP uart sample counter base

- **0:** bases on 16*baud_pulse, baud_rate = system clock frequency/16/divisor
- **1:**bases on 8*baud_pulse, baud_rate = system clock frequency/8/divisor
- **2**: bases on 4*baud_pulse, baud_rate = system clock frequency/4/divisor
- **3**: bases on step_count*baud_pulse, baud_rate = system clock frequency/step_count

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13MHz bases on different div_step value.

BAUD	DIV_STEP = 0	DIV_STEP = 1	DIV_STEP = 2
110	7386	14773	29545
300	2708	7386	14773
1200	677	2708	7386
2400	338	677	2708
4800	169	338	677
9600	85	169	338
19200	42	85	169
38400	21	42	85
57600	14	21	42
115200	7	14	21
230400	*	7	14
460800	*	*	7
921600	*	*	*

Table 22 Divisor needed to generate a given baud rate from 13MHz based on different div_step

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 26MHz bases on different div_step value.

BAUD	DIV_STEP = 0	DIV_STEP = 1	DIV_STEP = 2
110	14773	29545	59091
300	5417	14773	29545
1200	1354	5417	14773
2400	677	1354	5417
4800	339	677	1354
9600	169	339	667
19200	85	169	339
38400	42	85	169
57600	28	42	85
115200	14	28	42
230400	7	14	28
460800	*	7	14
921600	*	*	7

Table 23 Divisor needed to generate a given baud rate from 26MHz based on different div_step

+0024h STEP_COUNT STEP_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STEP_COUNT[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0							

When rate_step=3, the step count is the threshold value for uart sample counter (sample_num).

+0028h SAMPLE_COUNT SAMPLE_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPE_COUNT							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	‘hff							

When rate_step=3, uart gets the input data when sample_count=sample_num.

4.9 Real Time Clock

4.9.1 General Description

The Real Time Clock (RTC) module provides time and data information. It works on the 32.768KHz oscillator with independent power supply. When the MS is powered off, a dedicated regulator is used to supply the RTC block. If the main battery is not present, the backup supply such as a small mercury cell battery or a large capacitor is used. In addition to

provide timing data, alarm interrupt is generated and it can be used to power up the base-band core through the BBWAKEUP pin. Also, regulator interrupts corresponding to the seconds; minutes, hours and days can be generated whenever the time counter value reaches a maximum. The year span is supported up to 2127. The maximum day of month values are stored in the RTC block, which depend on the leap year condition.

4.9.2 Register Definitions

RTC+0000h Baseband power up RTC_BBPU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY_BBUP												AUTO	BBPU	WRITE_EN	PWREN
Type	W												R/W	R/W	R/W	R/W

KEY_BBPU Bus write acceptable only when KEY_BBPU = 0x43

AUTO If BBWAKEUP will be low state when SYSRST# high to low

- **0** BBWAKEUP won't be low state when SYSRST# high to low automatically
- **1** BBWAKEUP will be low state when SYSRST# high to low automatically

BBPU Controls the power of PMIC, when powerkey1=A357h & powerkey2=67D2h it will be the value programmed by software or it will be low if above situation is not true.

- **0** Power down
- **1** Power on

WRITE_EN When WRITE_EN is written as 0 by software program, the rtc write interface will be disabled until another system power on.

PWREN

- **0** RTC alarm has no action on power switch
- **1** When RTC alarm occurs, BBPU will be assigned as 1, then system power on by rtc alarm wakeup.

RTC+0004h RTC IRQ status RTC_IRQ_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TCSTA	ALSTA
Type															R/C	R/C

ALSTA This register indicates IRQ occurred due to alarm condition met

- **0** IRQ occurred for alarm condition met
- **1** No IRQ occurred for alarm condition met

TCSTA This register indicates IRQ occurred due to tick condition met

- **0** IRQ occurred for tick condition met
- **1** No IRQ occurred for tick condition met

RTC+0008h RTC IRQ enable RTC_IRQ_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ONESHOT	TC_EN	AL_EN
Type														R/W	R/W	R/W

ONESHOT Controls automatic reset of AL_EN & TC_EN

AL_EN This register indicates the control bit for IRQ generation due to alarm condition met

0 Disable IRQ generation due to alarm condition met

1 Enable the alarm time match interrupt. Clear it when ONESHOT is high upon generation of the corresponding IRQ

TC_EN This register indicates the control bit for IRQ generation due to tick condition met

0 Disable IRQ generation due to tick condition met

1 Enable the tick time match interrupt. Clear it when ONESHOT is high upon generation of the corresponding IRQ

RTC+000Ch Counter increment IRQ enable RTC_CII_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							1/8SEC CII	1/4SEC CII	1/2SEC CII	YEACI I	MTHC II	DOW CII	DOMC II	HOUC II	MINCII	SECC II
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.

SECCII Set this bit to 1 to activate the IRQ at each second update

MINCII Set the bit to 1 to activate the IRQ at each minute update

HOUCII Set the bit to 1 to activate the IRQ at each hour update

DOMCII Set the bit to 1 to activate the IRQ at each day of month update

DOWCII Set the bit to 1 to activate the IRQ at each day of week update

MTHCII Set the bit to 1 to activate the IRQ at each month update

YEACII Set the bit to 1 to activate the IRQ at each year update

1/2SECCII Set the bit to 1 to activate the IRQ at each one-half update

1/4SECCII Set the bit to 1 to activate the IRQ at each one-fourth update

1/8SECCII Set the bit to 1 to activate the IRQ at each one-eighth update

RTC+0010h RTC alarm mask RTC_AL_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										YEA_M SK	MTH_M SK	DOW_M SK	DOM_M SK	HOU_M SK	MIN_MS K	SEC_M SK
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm condition for alarm IRQ generation is according to each bit in this register is masked or not.

SEC_MSK

0 Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal

1 Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC won't affect the alarm IRQ generation

MIN_MSK

0 Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal

1 Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN won't affect the alarm IRQ generation

HOU_MSK

0 Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal

1 Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU won't affect the alarm IRQ generation

DOM_MSK

0 Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal

1 Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM won't affect the alarm IRQ generation

DOW_MSK

0 Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal

1 Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW won't affect the alarm IRQ generation

MTH_MSK

0 Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal

1 Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH won't affect the alarm IRQ generation

YEA_MSK

0 Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal

1 Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA won't affect the alarm IRQ generation

RTC+0014h RTC seconds time counter register RTC_TC_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND					
Type											R/W					

TC_SECOND The time counter second initial value. The range of its value is: 0-59.

RTC+0018h RTC minutes time counter register RTC_TC_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE					
Type											R/W					

TC_MINUTE The time counter minute initial value. The range of its value is: 0-59.

RTC+001Ch RTC hours time counter register RTC_TC_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR				
Type												R/W				

TC_HOUR The time counter hour initial value. The range of its value is: 0-23.

RTC+0x0020 RTC day of month time counter register RTC_TC_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_DOM				
Type												R/W				

TC_DOM The time counter day of month initial value. The day of month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

RTC+0x0024 RTC day of week time counter register RTC_TC_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW		
Type														R/W		

TC_DOW The time counter day of week initial value. The range of its value is: 1-7.

RTC+0x0028 RTC month time counter register RTC_TC_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH			
Type													R/W			

TC_MONTH The time counter month initial value. The range of its value is: 1-12.

RTC+0x002C RTC year time counter register RTC_TC_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AL_SECOND						
Type										R/W						

TC_YEAR The time counter year initial value. The range of its value is: 0-127. (2000-2127)

RTC+0x0030 RTC second alarm setting register RTC_AL_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_SECOND					
Type											R/W					

AL_SECOND The second value of the alarm counter setting. The range of its value is: 0-59.

RTC+0x0034 RTC minute alarm setting register RTC_AL_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_MINUTE					
Type											R/W					

AL_MINUTE The minute value of the alarm counter setting. The range of its value is: 0-59.

RTC+0x0038 RTC hour alarm setting register RTC_AL_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AL_HOUR				
Type												R/W				

AL_HOUR The hour value of the alarm counter setting. The range of its value is: 0-23.

RTC+0x003C RTC day of month alarm setting register RTC_AL_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AL_DOM				
Type												R/W				

AL_DOM The day of month value of the alarm counter setting. The day of month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

RTC+0x0040 RTC day of week alarm setting register RTC_AL_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AL_DOW		
Type														R/W		

AL_DOW The day of week value of the alarm counter setting. The range of its value is: 1-7.

RTC+0x0044 RTC month alarm setting register RTC_AL_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AL_MONTH			
Type													R/W			

AL_MONTH The month value of the alarm counter setting. The range of its value is: 1-12.

RTC+0x0048 RTC year alarm setting register RTC_AL_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AL_YEAR						
Type										R/W						

AL_YEAR The year value of the alarm counter setting. The range of its value is: 0-127. (2000-2127)

RTC+0x004C XOSC bias current control register RTC_XOSCCALI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												XOSCCALI				
Type												W				

XOSCCALI This register controls the XOSC32 bias current. Before the first program by software, the XOSCCALI value is 11111b.

RTC+0050h RTC_POWERKEY1 register RTC_POWERKEY1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY1															
Type	R/W															

RTC+0054h RTC_POWERKEY2 register RTC_POWERKEY2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY2															
Type	R/W															

These register sets are used to determine that if the real time clock has been programmed by software; i.e. the time value in real time clock is correct. When the real time clock first power on, the register contents are all in a mass, therefore the time values shown are incorrect. Software needs to know if the real time clock has been programmed. Hence, these two registers are defined for first power-on issue. After software programs the correct value, these two register sets don't need to be updated. In addition to program the correct time value, when contents of these register sets are wrong, the interrupt won't be generated; therefore, the real time clock won't generate the interrupts before software programs it. Unwanted interrupt due to wrong time value won't occur. The destined values of these two register sets are:

RTC_POWERKEY1 A357h
RTC_POWERKEY2 67D2h

RTC+0058h PDN1 RTC_PDN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_PDN1[7:0]							
Type									R/W							

RTC_PDN1[3:1] is for reset de-bounce mechanism.

- **0** 2ms
- **1** 8ms
- **2** 32ms
- **3** 128ms
- **4** 256ms
- **5** 512ms
- **6** 1024ms
- **7** 2048ms

RTC_PDN1[7:4] & RTC_PDN1[0] is the spare register for software to keep some power on and power off state information.

RTC+005Ch PDN2 RTC_PDN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_PDN2[7:0]							
Type									R/W							

RTC_PDN2 The spare register for software to keep some power on and power off state information.

4.10 Auxiliary ADC Unit

The auxiliary ADC unit is used to monitor the status of battery and charger, identify the plugged peripheral, and perform temperature measurement. There provides 5 input channels for diversified application in this unit.

There provides 2 modes of operation: immediate mode and timer-triggered mode. The mode of each channel can be individually selected through register AUXADC_CON0. For example, if the flag SYN0 in the register AUXADC_CON0 is set, the channel 0 will be set in timer-triggered mode. Otherwise, it's in immediate mode.

In immediate mode, the A/D converter will sample the value once only when the flag in the register AUXADC_CON1 has been set. For example, if the flag IMM0 in the register AUXADC_CON1 is set, the A/D converter will sample the data for channel 0. The IMM flags should be cleared and set again to initialize another sampling.

The value sampled for the channel 0 will be stored in the register AUXADC_DAT0, the value for the channel 1 will be stored in the register AUXADC_DAT1, and so on.

If the AUTOSET flag in the register AUXADC_CON3 is set, the auto-sample function is enabled. The A/D converter will sample the data for the channel for which the corresponding data register has been read. For example, in case the SYN1 flag is not set, and the AUTOSET flag is set, when the data register AUXADC_DAT0 has been read, the A/D converter will sample the next value for the channel 1 immediately.

If multiple channels are selected at the same time, the task will be performed sequentially on every selected channel. For example, if we set AUXADC_CON1 to be 0x1f, that is, all 5 channels are selected, the state machine in the unit will start sampling from channel 4 to channel 0, and save the values of each input channel in the respective registers. The same process also applies in the timer-triggered mode.

In timer-triggered mode, the A/D converter will sample the value for the channels for which the corresponding SYN flags are set when the TDMA timer counts to the value specified in the register TDMA_AUXEV1, which is placed in the TDMA timer. For example, if we set AUXADC_CON0 to be 0x1f, all 5 channels are selected to be in timer-triggered mode. The

state machine will make sampling for all 5 channels sequentially and save the values in registers from AUXADC_DAT0 to AUXADC_DAT4, as it does in immediate mode.

There provides a dedicated timer-triggered scheme for channel 0. The scheme is activated by setting the SYN5 flag in the register AUXADC_CON2. The timing offset for this event is stored in the register TDMA_AUXEV0 in the TDMA timer. The sampled data triggered by this specific event is stored in the register AUXADC_DAT5. It's used to separate the results of two individual software routines that perform action on the auxiliary ADC unit.

The AUTOCLR*n* in the register AUXADC_CON3 is set when it's intended to sample only once after setting timer-triggered mode. If AUTOCLR1 flag has been set, after the data for the channels in timer-triggered mode has been stored, the SYN*n* flags in the register AUXADC_CON0 will be cleared. Instead, if AUTOCLR0 flag has been set, after the data for the channel 0 has been stored in the register AUXADC_DAT5, the SYN5 flag in the register AUXADC_CON2 will be cleared.

The usage of the immediate mode and timer-triggered mode are mutual exclusive in terms of individual channel.

The PUWAIT_EN bit in the registers AUXADC_CON3 is used to power up the analog port in advance. That ensures that the power has ramped up to the stable state before A/D converter starts the conversion. The analog part will be automatically powered down after the conversion is completed.

4.10.1 Register Definitions

AUXADC+0000h Auxiliary ADC control register 0 AUXADC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SYN4	SYN3	SYN2	SYN1	SYN0
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

SYN*n* Those 5 bits define whether the corresponding channel is to be sampled or not in timer-triggered mode. It's associated with timing offset register TDMA_AUXEV1. It's supported to set multiple flags. The flags can be automatically clearly after those channel have been sampled if AUTOCLR1 in the register AUXADC_CON3 is set.

- **0** The channel is not selected.
- **1** The channel is selected.

AUXADC+0004h Auxiliary ADC control register 1 AUXADC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IMM4	IMM3	IMM2	IMM1	IMM0
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

IMM*n* Those 5 bits are set individually to sample the data for the corresponding channel. It's supported to set multiple flags.

- **0** The channel is not selected.
- **1** The channel is selected.

AUXADC+0008h Auxiliary ADC control register 2 AUXADC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SYN5
Type																R/W
Reset																0

SYN7 This bit is used only for channel 0 and to be associated with timing offset register TDMA_AUXEV0 in the TDMA timer in timer-triggered mode. The flag can be automatically clearly after channel 0 have been sampled if AUTOCLR0 in the register AUXADC_CON3 is set.

0 The channel is not selected.

1 The channel is selected.

AUXADC+000Ch Auxiliary ADC control register 3 AUXADC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET				PUWAIT_EN		AUTOCLR1	AUTOCLR0	TEST_DACMON	CALI						STA
Type	R/W				R/W		R/W	R/W	R/W	R/W						RO
Reset	0				0		0	0	0	0						0

AUTOSET The field defines the auto-sample mode of the module. In auto-sample mode, each channel with its sample register being read can start sampling immediately without configuring the control register AUXADC_CON1 again.

PUWAIT_EN The field enables the power warm-up period to ensure power stability before the SAR process take place. It's recommended to activate.

0 The mode is disabled.

1 The mode is enabled.

AUTOCLR1 The field defines the auto-clear mode of the module for event 1. In auto-clear mode, each timer-triggered channel get the samples of the specified channels once after the SYN*n* bit in the register AUXADC_CON0 have been set. The SYN*n* bits will be automatically be cleared and the channel will not being enabled again by the timer event except the SYN*n* flags are set again.

0 The automatic clear mode is not enabled.

1 The automatic clear mode is enabled.

AUTOCLR0 The field defines the auto-clear mode of the module for event 0. In auto-clear mode, the timer-triggered channel 0 get the sample once after the SYN5 bit in the register AUXADC_CON2 have been set. The SYN5 bit will be automatically cleared and the channel will not be enabled again by the timer event 0 except the SYN5 flag is set again.

0 The automatic clear mode is not enabled.

1 The automatic clear mode is enabled.

TEST_DACMON The field enables the test mode of the analog part.

0 The analog cell is in test mode.

1 The analog cell is in normal mode.

CALI The field defines the calibration value of the bias current for the analog part.

STA The field defines the state of the module.

0 This module is idle.

1 This module is operating.

AUXADC+0010h Auxiliary ADC channel 0 register AUXADC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DAT									
Type							RO									
Reset							0									

The register stores the sampled data for the channel 0. There are 6 registers of the same type for the corresponding channel. The overall register definition is listed in **Table 24**.

Register Address	Register Function	Acronym
AUXADC+0010h	Auxiliary ADC channel 0 data register	AUXADC_DAT0
AUXADC+0014h	Auxiliary ADC channel 1 data register	AUXADC_DAT1
AUXADC+0018h	Auxiliary ADC channel 2 data register	AUXADC_DAT2
AUXADC+001Ch	Auxiliary ADC channel 3 data register	AUXADC_DAT3
AUXADC+0020h	Auxiliary ADC channel 4 data register	AUXADC_DAT4
AUXADC+002Ch	Auxiliary ADC channel 0 data register for TDMA event 0	AUXADC_DAT5

Table 24 Auxiliary ADC data register list

4.11 Divider

To ease the processing load of MCU, a divider is employed here. The divider can operate signed and unsigned 32bit/32bit division, as well as modulus, and the processing time of the divider is from 1 clock cycle to 33 clock cycles, which is upon the magnitude of the value of the dividend. The detailed processing time is listed below in **Table 25**. From the table we can see that there are two kind of processing time, except the dividend is zero, in an item. That depends on the need of restoring at the last step of a division operation.

After the divider is started by setting START to "1" in Divider Control Register, DIV_RDY will go low, and it will be asserted after the division process is finished. MCU could detect this status bit by polling it to know the right access timing. In order to simplify the polling, only the value of register DIV_RDY will appear while Divider Control Register is read. Hence MCU doesn't need to mask other bits to extract the value of DIV_RDY.

In GSM/GPRS system, many divisions are executed with some constant divisors. Therefore, some often-used constants are stored in the divider to speed up the process. By controlling control bits IS_CNST and CNST_IDX in Divider Control register, one can start a division without giving a divisor. This could save the time for writing divisor in and the instruction fetch time thereof, and makes process more efficient.

Signed Division		Unsigned Division	
Dividend	**Clock Cycles**	**Dividend**	**Clock Cycles**
0000_0000h	1	0000_0000h	1
0000_00ffh – (-0000_0100h), excluding 0x0000_0000	8 or 9	0000_0001h – 0000_00ffh	8 or 9

0000_ffffh – (-0001_0000h)	16 or 17	0000_0100h – 0000_ffffh	16 or 17
00ff_ffffh – (-0100_0000h)	24 or 25	0001_0000h – 00ff_ffffh	24 or 25
7fff_ffffh – (-8000_0000h)	32 or 33	0100_0000h – ffff_ffffh	32 or 33

Table 25 Processing time in different value of dividend.

4.11.1 Register Definitions

DIVIDER+0000h Divider Control Register DIV_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CNST_IDX							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IN_CNST	SIGN			DIV_RDY	START
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W	W	R/W	R/W	R	W
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

START To start division. It will return to 0 after division is started.

DIV_RDY Current status of divider. Note that when DIV_CTRL register is read, only the value of DIV_RDY will appear. That means program doesn't need to mask other part of the register to extract the information of DIV_RDY.

- **0** division is in progress.
- **1** division is finished.

SIGN To indicate signed or unsigned division.

- **0** Unsigned division.
- **1** Signed division.

IS_CNST To indicate if use internal constant value as a divisor. If IS_CNST is enabled, User needn't to write value of divisor, and divider will automatically use internal constant value instead. What value divider will use is according to the value of CNST_IDX.

- **0** Normal division. Divisor is written in via APB
- **1** Using internal constant divisor instead.

CNST_IDX Index of constant divisor.

- **0** divisor = 13
- **1** divisor = 26
- **2** divisor = 51
- **3** divisor = 52
- **4** divisor = 102
- **5** divisor = 104

DIVIDER +0004h Divider Dividend register DIV_DIVIDEND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIVIDEND[31:16]															
Type	W															
Reset	0															

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVIDEND[15:0]															
Type	W															
Reset	0															

Dividend.

DIVIDER +0008h Divider Divisor register DIV_DIVISOR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIVISOR[31:16]															
Type	W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVISOR[15:0]															
Type	W															
Reset	0															

Divisor.

DIVIDER +000Ch Divider Quotient register DIV_QUOTIENT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QUOTIENT[31:16]															
Type	R															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QUOTIENT[15:0]															
Type	R															
Reset	0															

Quotient.

DIVIDER +0010h Divider Remainder register DIV_REMAINDER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REMAINDER[31:16]															
Type	R															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REMAINDER[15:0]															
Type	R															
Reset	0															

Remainder.

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4.12 CSD Accelerator

4.12.1 General Description

This unit performs the data format conversion of RA0 RA1 and FAX in CSD service. CSD service comprises two major functions, data flow throttling and data format conversion. The data format conversion is a bit-base operation and takes a number of instructions to complete a conversion. Therefore it's not efficient to do by MCU self. A coprocessor, CSD accelerator, is designed here to reduce the computing power need by performing this function.

What CSD accelerator do is just help to convert data format, and the function of data flow throttling is still implemented by MCU. Basically, CSD accelerator performs three types of data format conversion, RA0, RA1 and FAX.

For RA0 conversion, only uplink RA0 data format conversion is provided here. That's because there are too many judgments on downlink path conversion, and this will greatly increase area cost. Uplink RA0 conversion is to insert one start bit and one stop bit before and after a byte respectively during 16 bytes. **Figure 29** illustrates the detailed conversion table.

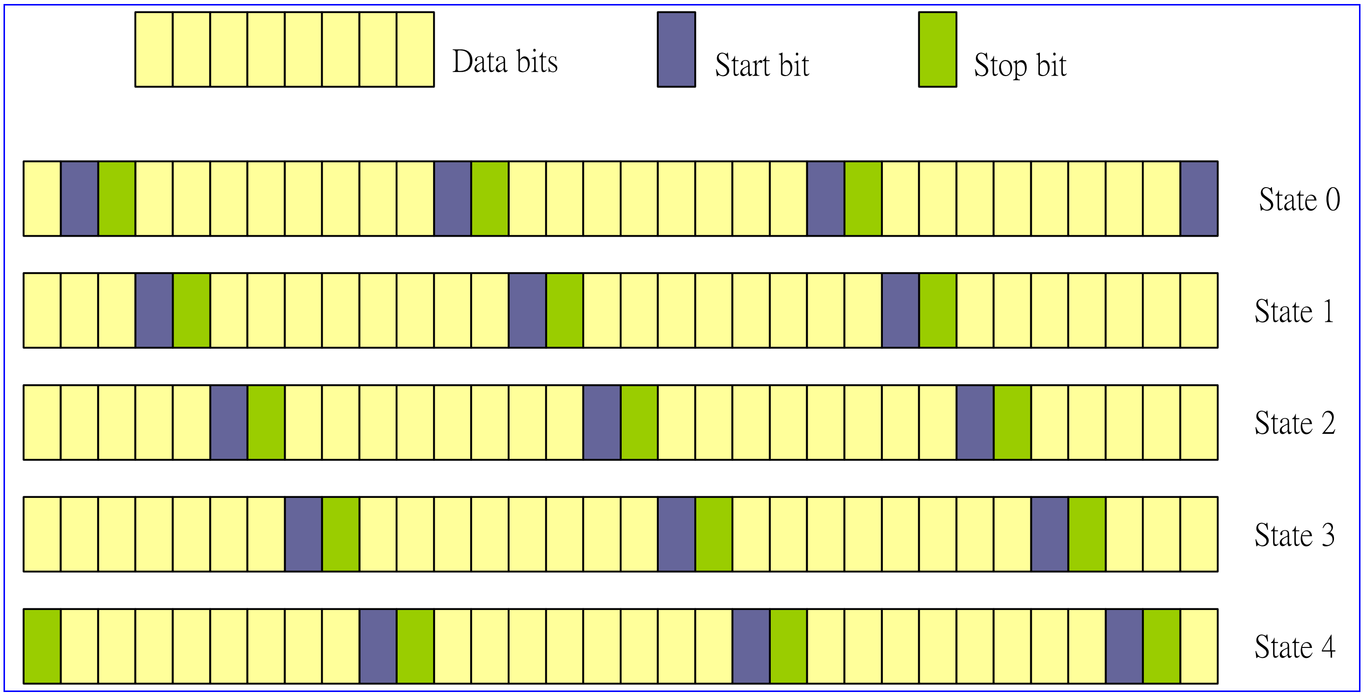

Figure 29 data format conversion of RA0

For RA1 conversion, both directions, downlink and uplink, are supported. The data formats vary in different data rate. The detailed conversion table is shown in **Figure 30** and **Figure 31**. The yellow part is the payload data, and the blue part is status bit.

Bit 0 → Bit 6

D1	D2	D3	D4	D5	D6	S1
D7	D8	D9	D10	D11	D12	X
D13	D14	D15	D16	D17	D18	S3
D19	D20	D21	D22	D23	D24	S4
E4	E5	E6	E7	D25	D26	D27
D28	D29	D30	S6	D31	D32	D33
D34	D35	D36	X	D37	D38	D39
D40	D41	D42	S8	D43	D44	D45
D46	D47	D48	S9			

Bit 59

Figure 30 data format conversion for 6k/12k RA1

Bit 0 → Bit 7

D1	D2	D3	S1	D4	D5	D6	X
D7	D8	D9	S3	D10	D11	D12	S4
E4	E5	E6	E7	D13	D14	D15	S6
D16	D17	D18	X	D19	D20	D21	S8
D22	D23	D24	S9				

Bit 36

Figure 31 data format conversion for 3.6k RA1

For FAX, two types of bit-reversal functions are provided. One is bit-wise reversal, and the other is byte-wise reversal, which are illustrated in **Figure 32** and **Figure 33** respectively.

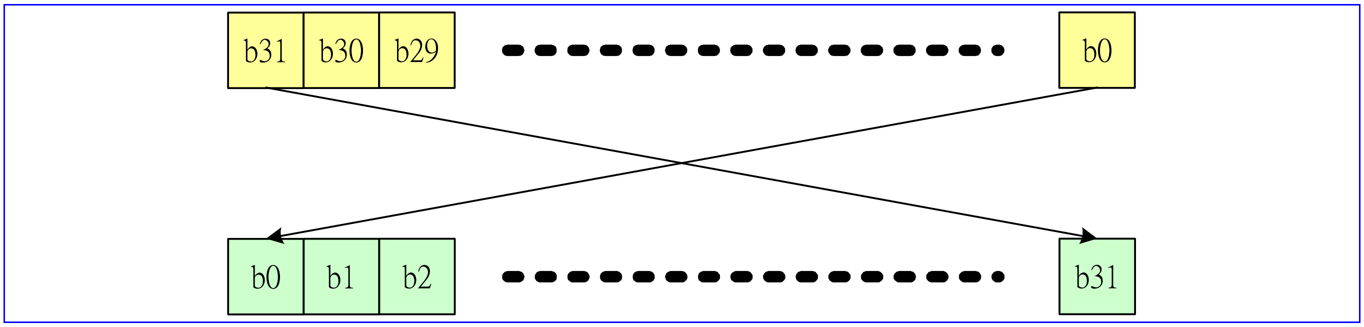

Figure 32 Type 1 bit reverse

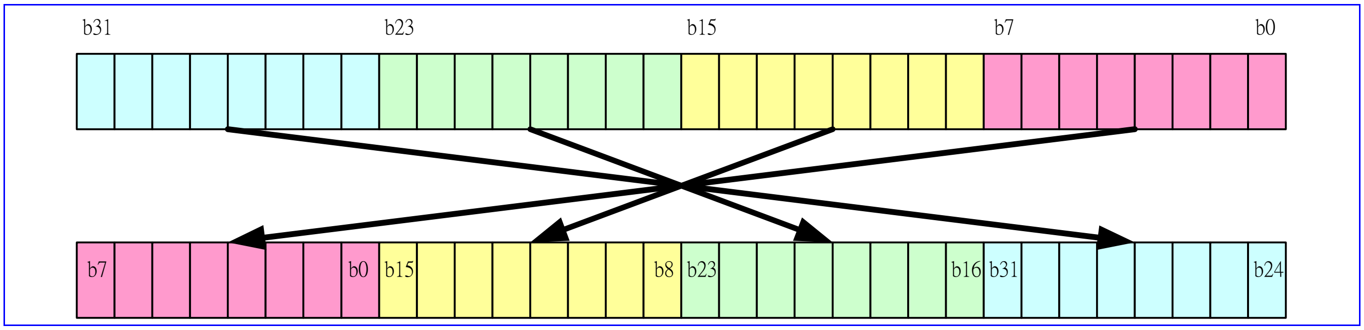

Figure 33 Type 2 bit reverse

Register Address	Register Function	Acronym
CSD + 0000h	CSD RA0 Control Register	**CSD_RA0_CON**
CSD + 0004h	CSD RA0 Status Register	**CSD_RA0_STA**
CSD + 0008h	CSD RA0 Input Data Register	**CSD_RA0_DI**
CSD + 000Ch	CSD RA0 Output Data Register	**CSD_RA0_DO**
CSD + 0100h	CSD RA1 6K/12K Uplink Input Data Register 0	**CSD_RA1_6_12K_ULDI0**
CSD + 0104h	CSD RA1 6K/12K Uplink Input Data Register 1	**CSD_RA1_6_12K_ULDI1**
CSD + 0108h	CSD RA1 6K/12K Uplink Status Data Register	**CSD_RA1_6_12K_ULSTUS**
CSD + 010Ch	CSD RA1 6K/12K Uplink Output Data Register 0	**CSD_RA1_6_12K_ULDO0**
CSD + 0110h	CSD RA1 6K/12K Uplink Output Data Register 1	**CSD_RA1_6_12K_ULDO1**
CSD + 0200h	CSD RA1 6K/12K Downlink Input Data Register 0	**CSD_RA1_6_12K_DLDI0**
CSD + 0204h	CSD RA1 6K/12K Downlink Input Data Register 1	**CSD_RA1_6_12K_DLDI1**
CSD + 0208h	CSD RA1 6K/12K Downlink Output Data Register 0	**CSD_RA1_6_12K_DLDO0**
CSD + 020Ch	CSD RA1 6K/12K Downlink Output Data Register 1	**CSD_RA1_6_12K_DLDO1**
CSD + 0210h	CSD RA1 6K/12K Downlink Status Data Register	**CSD_RA1_6_12K_DLSTUS**
CSD + 0300h	CSD RA13.6K Uplink Input Data Register 0	**CSD_RA1_3P6K_ULDI0**
CSD + 0304h	CSD RA13.6K Uplink Status Data Register	**CSD_RA1_3P6K_ULSTUS**
CSD + 0308h	CSD RA13.6K Uplink Output Data Register 0	**CSD_RA1_3P6K_ULDO0**
CSD + 030Ch	CSD RA13.6K Uplink Output Data Register 1	**CSD_RA1_3P6K_ULDO1**
CSD + 0400h	CSD RA1 3.6K Downlink Input Data Register 0	**CSD_RA1_3P6K_DLDI0**
CSD + 0404h	CSD RA1 3.6K Downlink Input Data Register 1	**CSD_RA1_3P6K_DLDI1**

CSD + 0408h	CSD RA1 3.6K Downlink Output Data Register 0	**CSD_RA1_3P6K_DLDO0**
CSD + 040Ch	CSD RA1 3.6K Downlink Status Data Register	**CSD_RA1_3P6K_DLSTUS**
CSD + 0500h	CSD FAX Bit Reverse Type 1 Input Data Register	**CSD_FAX_BR1_DI**
CSD + 0504h	CSD FAX Bit Reverse Type 1 Output Data Register	**CSD_FAX_BR1_DO**
CSD + 0510h	CSD FAX Bit Reverse Type 2 Input Data Register	**CSD_FAX_BR2_DI**
CSD + 0514h	CSD FAX Bit Reverse Type 2 Output Data Register	**CSD_FAX_BR2_DO**

Table 26 CSD Accelerater Registers

4.12.2 Register Definitions

CSD+0000h CSD RA0 Control Register CSD_RA0_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name											RST	BTS0		VLD_BYTE		
Type											W	W		R/W		
Reset											0	0		100		

VLD_BYTE Specify how many valid bytes of current input data. It must be specified before filling data in.

BTS0 Back to state 0. Force RA0 converter go back to state 0. Incomplete word will be padded by STOP bit. For instance, back-to-state0 command is issued after 8 byte data are filled in. Then these bit after the 8th byte will be padded with stop bits, and RDYWD2 is asserted. After removing state word 2, the state pointer goes back to state 0. Note that new data filling should take place after removing state word 2, or the state pointer may be out of order.

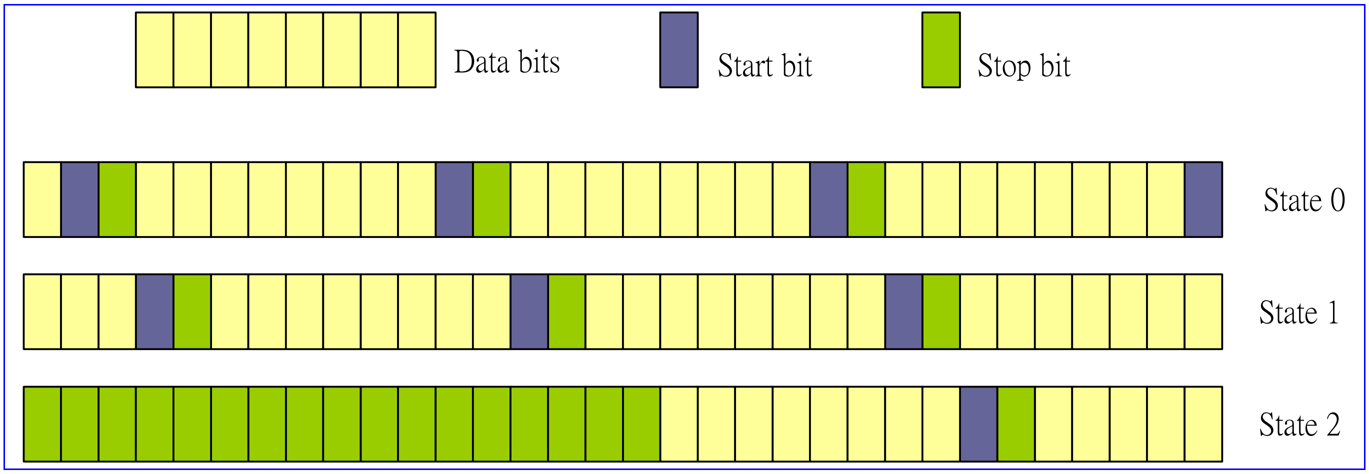

Figure 34 Example of Back to state 0

RST Reset RA0 converter. In case, erroneously operation makes data disordered. This bit can restore all state to original state.

CSD+0004h CSD RA0 Status Register CSD_RA0_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BYTECNT				CRTSTA			RDYWD				
Type					R/W				R/W			RC				
Reset					0				0			0				

RDYWD0~4 Ready word. To indicate which state word is ready for withdrawal. Data should be withdrawn before next data filling into CSD_RA0_DI, if there are any bits asserted.

0 Not ready

1 Ready

CRTSTA current state. State0 ~ state4. To indicate which state word software is filling in.

BYTECNT The total number of bytes software filling in.

CSD+0008h CSD RA0 Input Data Register CSD_RA0_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The RA0 convert input data. Ready word indicator shall be check before filling in data. If there are any words ready, withdraw them first, or the ready data in RA0 converter will be replaced.

CSD+000Ch CSD RA0 Output Data Register CSD_RA0_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT RA0 converted data. The return data is corresponding to the ready word indicator defined in CSD_RA0_STA register. The five bit of RDYWD map to state0 ~ state 4 accordingly. When CSD_RA0_DO is read, the asserted state word will be returned. If there are two state words asserted at the same time, the lower one will be returned.

CSD+0100h CSD RA1 6K/12K Uplink Input Data Register 0 CSD_RA1_6_12K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	DIN
Type	R/W
Reset	0

DIN The D1 to D32 of RA1 uplink data.

CSD+0104h CSD RA1 6K/12K Uplink Input Data Register 1 CSD_RA1_6_12K_ULDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The D33 to D48 of RA1 uplink data.

CSD+0108h CSD RA1 6K/12K Uplink Status Data Register CSD_RA1_6_12K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

SA Represents S1, S3, S6, and S8 of status bits.
SB Represents S4 and S9 of status bits.
X Represents X of status bits.
E4 Represents E4 of status bits.
E5 Represents E5 of status bits.
E6 Represents E6 of status bits.
E7 Represents E7 of status bits.

CSD+010Ch CSD RA1 6K/12K Uplink Output Data Register 0 CSD_RA1_6_12K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOU															
Type	R/W															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 6K/12K uplink frame.

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CSD+0110h CSD RA1 6K/12K Uplink Output Data Register 1 CSD_RA1_6_12K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DOUT											
Type					R/W											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT The bit32 to bit 59 of RA1 6K/12K uplink frame.

CSD+0200h CSD RA1 6K/12K Downlink Input Data Register 0 CSD_RA1_6_12K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The bit 0 to bit 31 of RA1 6K/12K downlink frame.

CSD+0204h CSD RA1 6K/12K Downlink Input Data Register 1 CSD_RA1_6_12K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DIN											
Type					R/W											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The bit32 to bit 59 of RA1 6K/12K downlink frame.

CSD+0208h CSD RA1 6K/12K Downlink Output Data Register 0 CSD_RA1_6_12K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT The D1 to D32 of RA1 downlink data.

CSD+020Ch CSD RA1 6K/12K Downlink Output Data Register 1 CSD_RA1_6_12K_DLDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT The D33 to D48 of RA1 downlink data.

CSD+0210h CSD RA1 6K/12K Downlink Status Data Register CSD_RA1_6_12K_DLSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.

SB The result of majority votes of S4 and S9. SB is “0” if equal vote.

X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0300h CSD RA1 3.6K Uplink Input Data Register 0 CSD_RA1_3P6K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DIN							
Type									R/W							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The D1 to D24 of RA1 3.6K uplink data.

CSD+0304h CSD RA1 3.6K Uplink Status Data Register CSD_RA1_3P6K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

SA Represents S1, S3, S6, and S8 of status bits.

SB Represents S4 and S9 of status bits.

X Represents X of status bits.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0308h CSD RA1 3.6K Uplink Output Data Register 0 CSD_RA1_3P6K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 3.6K uplink frame

CSD+030Ch CSD RA1 3.6K Uplink Output Data Register 1 CSD_RA1_3P6K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DOUT			
Type													R/W			
Reset													0			

DOUT The bit 32 to bit 35 of RA1 3.6K uplink frame

CSD+0400h CSD RA1 3.6K Downlink Input Data Register 0 CSD_RA1_3P6K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN The bit 0 to bit 31 of RA1 3.6K downlink frame

CSD+0404h CSD RA1 3.6K Downlink Input Data Register 1 CSD_RA1_3P6K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DIN			
Type													R/W			
Reset													0			

DIN The bit 32 to bit 35 of RA1 3.6K downlink frame

CSD+0408h CSD RA1 3.6K Downlink Output Data Register 0 CSD_RA1_3P6K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DOUT							
Type									R/W							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DIN The D1 to D24 of RA1 3.6K downlink data.

CSD+040Ch CSD RA1 3.6K Downlink Status Data Register CSD_RA1_3P6K_DLSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.

SB The result of majority votes of S4 and S9. SB is “0” if equal vote.

X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0500h CSD FAX Bit Reverse Type 1 Input Data Register CSD_FAX_BR1_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															

Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN 32-bit input data for type 1 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by word.

CSD+0504h CSD FAX Bit Reverse Type 1 Output Data Register CSD_FAX_BR1_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT 32-bit result data for type 1 bit reverse of FAX data.

CSD+0510h CSD FAX Bit Reverse Type 2 Input Data Register CSD_FAX_BR2_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	R/W															
Reset	0															

DIN 32-bit input data for type 2 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by byte.

CSD+0514h CSD FAX Bit Reverse Type 2 Output Data Register CSD_FAX_BR2_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	R/W															
Reset	0															

DOUT 32-bit result data for type 2 bit reverse of FAX data.

5 Audio Front-end

5.1 General Description

The audio front-end is a part of the voice band data path. The whole voice band data paths are complied with GSM 03.50 specification. The audio front-end is mainly composed of two parts. The first part is the up-link path, which interfaces with the input microphone (or the other auxiliary input device) and the DSP. And the second part is the downlink path, which interfaces with the DSP and the output earphone (or the other auxiliary output device). Besides, there is a Digital Audio Interface (DAI) block to communicate with the System Simulator for FTA. **Figure 35** is the block diagram of the audio front-end.

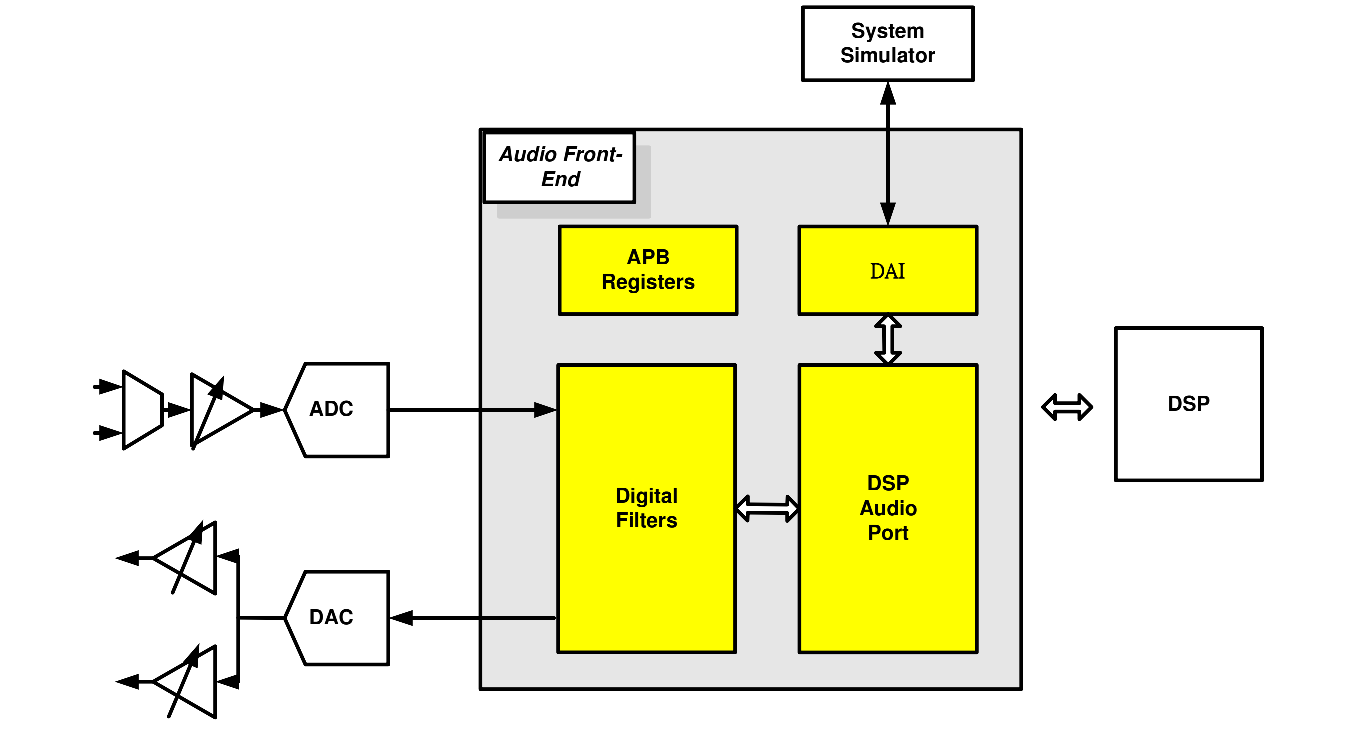

Figure 35 Block diagram of audio front-end.

The up-link voice data path includes the following blocks:

- One 2-input multiplexer to choose the input signal sources fed into up-link LNA.
- One LNA for microphone or auxiliary input device. It features a programmable gain controlled by VUPG[3:0] of AFE_AG_CON with steps of 3dB. The gain settings on VUPG[3:0] are shown in the **Table 27** and **Table 28**.
- A 2nd order sigma-delta modulator with over sampling ratio of 512, with two level (1 bit) or three level (2 bits) output at 4096-KHz. The sigma-delta modulator will provide analog to digital conversion with sufficient dynamic range and signal-to-noise ratio.
- Digital filters perform signal decimation and band-limits the digital data to specified signal bandwidth (300-3400 Hz) with sufficiently attenuation.

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- A 30-tap compensation filter is implemented in DSP algorithm to cope with acoustic effect.

VUPG[3:0]	Gain(dBm0/dBVrms)
1111	55.58
1110	52.58
1101	49.58
1100	46.58
1011	43.58
1010	40.58
1001	37.58
1000	34.58
0111	31.58
0110	28.58
0101	25.58
0100	22.58
0011	19.58
0010	16.58
0001	13.58
0000	10.58

Table 27 VUPG[3:0] gain settings (VCFG[2] = '0').

VUPG[3:0]	Gain(dBm0/dBVrms)
X111	-10.42
X110	-7.42
X101	-4.42
X100	-1.42
X011	1.58
X010	4.58
X001	7.58
X000	10.58

Table 28 VUPG[3:0] gain settings (VCFG[2] = '1').

The down-link voice data path includes the following blocks:

- A 30-tap compensation filter and a digital gain stage are reserved in DSP algorithm to cope with acoustic effect.
- Digital filters perform signal interpolation and band-limits the digital data to specified signal bandwidth (300-3400 Hz) with sufficiently attenuation..
- A digital Sigma-Delta modulator pushes the in-band quantization noise to high frequency band and thus reduces the in-band quantization noise.
- A digital-to-analog interface converting the bit-stream data to analog format.

- A second order analog smoothing-filter attenuates the high-frequency noise generated by the sigma-delta modulator.
- Two differential output buffer for external speaker of 28Ω minimum impedance. They feature programmable gains controlled by VDPG0[3:0]/VDPG1[3:0] of AFE_AG_CON with steps of 2-dB. The gain settings on VDPG0[3:0]/VDPG1[3:0] are shown in **Table 29**.

VDPG1/0[3:0]	Gain(dBm0/dBVrms)
1111	3.39
1110	1.39
1101	-0.61
1100	-2.61
1011	-4.61
1010	-6.61
1001	-8.61
1000	-10.61
0111	-12.61
0110	-14.61
0101	-16.61
0100	-18.61
0011	-20.61
0010	-22.61
0001	-24.61
0000	-26.61

Table 29 VDPG1/0[3:0] gain settings.

5.2 Register Definitions

MCU APB bus registers in audio front-end are listed as followings.

AFE+0000h[MCU] AFE MCU Control Register — AFE_MCU_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VAFE ON
Type																R/W
Reset																0

MCU sets this register to start audio front-end operation. A synchronous reset signal will be issued. Then periodical interrupts of 8-KHz frequency will be issued. Clear this register will stop the interrupt.

VAFEON turn on audio front-end operations

AFE +0004h[MCU] AFE Analog Gain Control Register AFE_AG_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VUPG 3	VUPG 2	VUPG 1	VUPG 0	VDPG 0 3	VDPG 0 2	VDPG 0 1	VDPG 0 0	VDPG 1 3	VDPG 1 2	VDPG 1 1	VDPG 1 0
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Set this register for analog PGA gains. VUPG is set for microphone input volume control. And VDPG0 and VDPG1 are set for two output volume controls

VUPG[3:0] voice-band up-link PGA gain control bits
VDPG0[3:0] voice-band down-link PGA0 gain control bits
VDPG1[3:0] voice-band down-link PGA1 gain control bits

AFE +0008h[MCU] AFE Analog-Circuit Control Register 0 AFE_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						VCFG 3	VCFG 2	VCFG 1	VCFG 0	VDSE ND1	VDSE ND0	VCALI 4	VCALI 3	VCALI 2	VCALI 1	VCALI 0
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

Set this register for analog circuit configuration controls. Please refer to analog functional specification for details

VCFG[3:0] input interface configuration control
VDSEND[1:0] single-ended configuration control for out1 and out0
VCALI[4:0] biasing current control

AFE +000Ch[MCU] AFE Analog-Circuit Control Register 1 AFE_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBG_ CTRL 1	VBG_ CTRL 0	VPDN _CHP UMP	VFLO AT	VRSD ON	VRES SW	VLNAI NMOD E	VADC INMO DE1	VADC INMO DE0	VADC OUTM ODE	VDAC INMO DE 1	VDAC INMO DE0
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Set this register for analog circuit configuration controls. There are several loop back modes and test modes implemented for test purposes. Please refer to analog functional specification for details. Default values correspond to the normal function mode

VBG_CTRL[1:0] voice-band band-gap control
VPDN_CHPUMP voice-band charge pump power down
- **0**: power down (normal operating mode)
- **1**: charge pump on (for fab. process)

VFLOAT voice-band output driver float
- **0**: normal operating mode
- **1**: float mode

VRSDON voice-band redundant signed digit function on

0: 1-bit 2-level mode

1: 2-bit 3-level mode

VRESSW voice-band output buffer 1 output DC voltage control.

VLNAINMODE voice-band (uplink) LNA input mode(reserved).

VADCINMODE[1:0] Voice-band A/D input mode.

00: normal operating mode

01: the A/D input from the DAC output

10: N/A

11: N/A

VADCOUTMODE Voice-band A/D output mode.

0: N/A

1: N/A

VDACINMODE[1:0] Voice-band D/A input mode.

00: normal operating mode

01: N/A

10: the DAC input from the A/D output

11: the DAC input from the A/D output

AFE +0010h^MCU AFE Analog Power Down Control Register AFE_APDN_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PDN_ANA	PDN_BIAS	PDN_LNA	PDN_ADC	PDN_DAC	PDN_OUT1	PDN_OUT0
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

Set this register to power up analog blocks. Note that PDN_ANA gates all other register bits. 0: power down, 1: power up.

PDN_ANA all analog blocks

PDN_BIAS bias block

PDN_LNA low noise amplifier block

PDN_ADC ADC block

PDN_DAC DAC block

PDN_OUT1 OUT1 buffer block

PDN_OUT0 OUT0 buffer block

AFE +0014h^MCU AFE DAI Control Register AFE_DAI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VDAION					
Type											R/W					
Reset											0					

Set this register for DAI test mode

VDAION DAI function on

AFE +0018h[MCU] AFE Look-Back mode Control Register AFE_LB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													VBYPASSIIR	VDAPINMODE	VINTINMODE	VDECINMODE
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

Set this register for digital circuit configuration control. There are several loop back modes implemented for test purposes. Default values correspond to the normal function mode

VBYPASSIIR bypass hardware IIR filters

VDAPINMODE DSP audio port input mode control

0: normal mode

1: loop back mode

VINTINMODE interpolator input mode control

0: normal mode

1: loop back mode

VDECINMODE decimator input mode control

0: normal mode

1: loop back mode

5.3 Programming Guide

There are several cases, including speech call, voice memo record, voice memo playback, melody playback and DAI tests, partial or whole audio front-end need to be turned on. Followings are audio front-end programming procedures recommended to turn on audio front-end:

- MCU programs the AFE_DAI_CON, AFE_LB_CON, AFE_AG_CON, AFE_AC_CON0, AFE_AC_CON1 and AFE_APDN_CON for specific operation modes.
- MCU clear AFE bit of PDN_CON2 in software power down control register to power up audio front-end.
- MCU set AFE_MCU_CON to start the operation of audio front-end.

Followings are audio front-end programming procedures recommended to turn off audio front-end:

- MCU clear AFE_MCU_CON to stop the operation of audio front-end.
- MCU programs AFE_APDN_CON to power down AFE.
- MCU set AFE bit of PDN_CON2 in software power down control register to gate the clock and enables for audio front-end.

To start the DAI test, the MS firstly receives a GSM Layer 3 TEST_INTERFACE message from the SS and puts the speech transcoder into one of the following modes:

- Normal mode (VDAIMODE[1:0]: 00)
- Test of speech encoder/DTX functions (VDAIMODE[1:0]: 10)

- Test of speech decoder/DTX functions (VDAIMODE[1:0]: 01)
- Test of acoustic devices and A/D & D/A (VDAIMODE[1:0]: 11)

Then waits for DAIRST# signaling from the SS. Recognizing this, DSP starts to transmit to and/or receive from DSP Audio Port. For more detail, please refer to GSM 11.10 specification.

6 Radio Interface Control

This chapter details the MT6205B interface control with the radio part of a GSM terminal. Providing a comprehensive control scheme, the MT6205B radio interface consists of Baseband Serial Interface (BSI), Baseband Parallel Interface (BPI), Automatic Power Control (APC) and Automatic Frequency Control (AFC) together with APC-DAC and AFC-DAC.

6.1 Base-band Serial Interface

The Base-band Serial Interface is used to control the external radio components. It utilizes a 3-wire serial bus to transfer data to RF circuitry for PLL frequency change, reception gain setting, and other radio control purposes. In this unit, BSI data registers are double-buffered in the same way as the TDMA event registers. The MCU writes data into the write buffer and the data is transferred from the write buffer to the active buffer when TDMA_EVTVAL signal from the TDMA timer is pulsed.

Each data register BSI_Dx_DAT is associated with one data control register BSI_Dx_CON. It is used to identify which events (signaled by TDMA_BSI) generated by the TDMA timer would trigger the download process of the word through the serial bus, as well as the length of the word in bits. A special event is defined. The event is triggered by the operation that the MCU writes 1 to the IMOD flag. It provides immediate download process without programming the TDMA timer.

If more than one data word is to be downloaded on the same event, the word with the lowest address among them will be downloaded first, followed by the next lowest and so on.

The total time to download the words depends on the word length, the number of words to download, and the clock rates. The programmer should space the successive event to provide enough time. If the download process of the previous event isn’t complete before the new events come, the later will be suppressed.

The unit supports 2 external components. There are four output pins. BSI_CLK is the output clock, BSI_DATA is the serial data port, and BSI_CS0 and BSI_CS1 are the select pins for 2 components, respectively. BSI_CS1 is multiplexed with other function. To enable it, the mode control field (GPIObase+24)[16:15] should be set to 10. Note that BSI_CS1 of the BSI and BPI_BUS7 couldn’t be used simultaneously.

The block diagram of the BSI unit is as depicted in **Figure 36**.

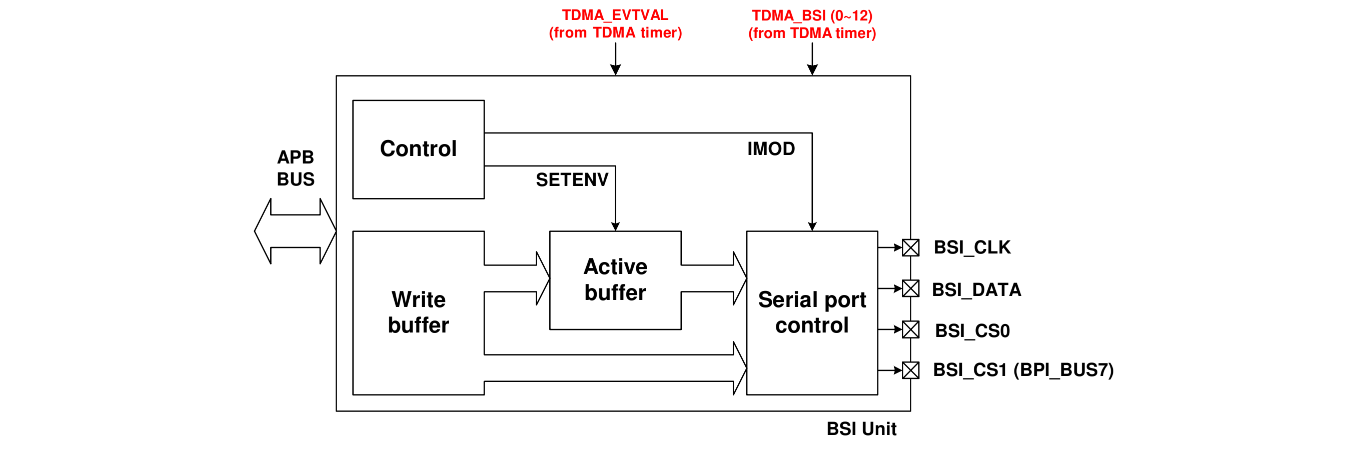

Figure 36 Block diagram of BSI unit.

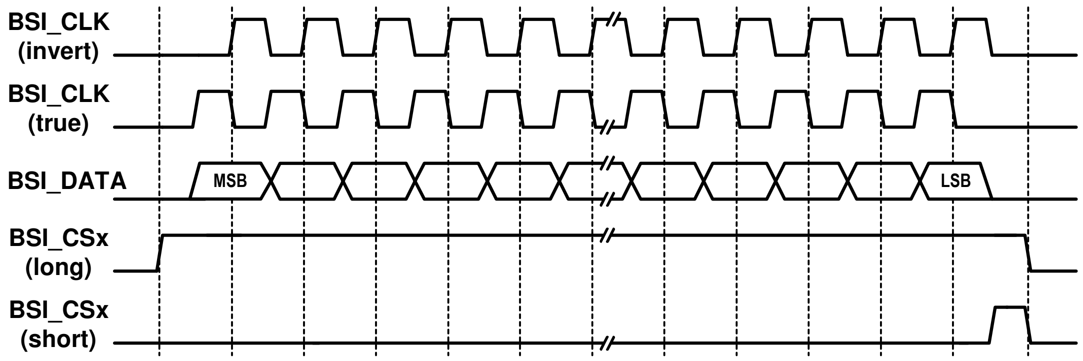

Figure 37 Timing characteristic of BSI interface

6.1.1 Register Definitions

BSI+0000h BSI control register BSI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SETENV	EN1_POL	EN1_LEN	EN0_POL	EN0_LEN	IMOD	CLK_SPD		CLK_POL
Type								R/W	R/W	R/W	R/W	R/W	WO	R/W		R/W
Reset								0	0	0	0	0	N/A	0		0

This register is the control register of the BSI unit. It controls the signal type of the 3-wire interface.

CLK_POL The flag controls the polarity of BSI_CLK. Refer to **Figure 37**.

- **0** True clock polarity
- **1** Inverted clock polarity

CLK_SPD The field defines the clock rate of BSI_CLK. The 3-wire interface provides 4 rates. The default is 13/2 MHz.

- **00** 13/2 MHz
- **01** 13/4 MHz
- **10** 13/6 MHz
- **11** 13/8 MHz

IMOD The field enables the immediate mode. If the MCU writes 1 to the flag, the download will be triggered immediately without waiting for the timer events. The words in which the event ID equals to 1fh will be downloaded following this signal. This flag is write-only. The immediate write can be exercised once. That means the programmer should write the flag again to start another immediate downloading. Setting the flag won't disable the other events from the timer. In case it's required to turn off all the events, the programmer can disable them by setting BSI_ENA to all zero.

ENX_LEN The field controls the type of the signal BSI_CS0 and BSI_CS1. Refer to **Figure 37**.

- **0** Long enable pulse
- **1** Short enable pulse

ENX_POL The field controls the polarity of the signal BSI_CS0 and BSI_CS1.

- **0** True enable pulse polarity
- **1** Inverted enable pulse polarity

SETENV The flag enables the write operation of the active buffer.

- **0** The MCU writes to the write buffer. The data is then latched in the active buffer after TDMA_EVTVAL is pulsed

1 The MCU directly write data to the active buffer.

BSI+0004h Data register control BSI_D0_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISB			LEN								EVT_ID				
Type	R/W			R/W								R/W				

The register is the control register of the data 0. It decides the length of the downloadable data word, the event to trigger the download process of the word, and which device it targets.

EVT_ID This field stores the event ID that the data word is due to be downloaded.

00000~01100 Synchronously download of the word with the selected EVT_ID event. The match between this field and the event is listed as **Table 25**.

EVT_ID	Event name
00000	TDMA_BSI0
00001	TDMA_BSI1
00010	TDMA_BSI2
00011	TDMA_BSI3
00100	TDMA_BSI4
00101	TDMA_BSI5
00110	TDMA_BSI6
00111	TDMA_BSI7
01000	TDMA_BSI8
01001	TDMA_BSI9
01010	TDMA_BSI10
01011	TDMA_BSI11
01100	TDMA_BSI12

Table 30 The match between the value of EVT_ID field in the BSI control registers and the TDMA_BSI events.

01101~11110 Reserved

11111 Immediate download

LEN The field stores the length of the data word. The actual length is defined as LEN + 1 in units of bits. The value ranges from 0 to 31, corresponding to 1 to 32 bits in length.

ISB The flag selects the target device.

0 Device 0 is selected.

1 Device 1 is selected.

BSI +0008h Data register BSI_D0_DAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT [15:0]															
Type	R/W															

DAT Data part of the word

BSI +0190h BSI event enable register BSI_ENA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

The register could enable the event by setting the corresponding bit. After hardware reset, all bits are initialized as 1. Besides, those bits are set as 1 after TDMA_EVTVAL is pulsed.

BSIx The flag enables the downloading of the words that corresponds to the events signaled by TMDA_BSI.

- **0** The event is not enabled.
- **1** The event is enabled.

There are totally 22 pairs of data registers. The address mapping and function is listed as **Table 31**.

Register Address	Register Function	Acronym
BSI +0004h	Control part of data register 0	BSI_D0_CON
BSI +0008h	Data part of data register 0	BSI_D0_DAT
BSI +000Ch	Control part of data register 1	BSI_D1_CON
BSI +0010h	Data part of data register 1	BSI_D1_ DAT
BSI +0014h	Control part of data register 2	BSI_D2_CON
BSI +0018h	Data part of data register 2	BSI_D2_ DAT
BSI +001Ch	Control part of data register 3	BSI_D3_CON
BSI +0020h	Data part of data register 3	BSI_D3_ DAT
BSI +0024h	Control part of data register 4	BSI_D4_CON
BSI +0028h	Data part of data register 4	BSI_D4_ DAT
BSI +002Ch	Control part of data register 5	BSI_D5_CON
BSI +0030h	Data part of data register 5	BSI_D5_ DAT
BSI +0034h	Control part of data register 6	BSI_D6_CON
BSI +0038h	Data part of data register 6	BSI_D6_ DAT
BSI +003Ch	Control part of data register 7	BSI_D7_CON
BSI +0040h	Data part of data register 7	BSI_D7_ DAT
BSI +0044h	Control part of data register 8	BSI_D8_CON
BSI +0048h	Data part of data register 8	BSI_D8_ DAT
BSI +004Ch	Control part of data register 9	BSI_D9_CON
BSI +0050h	Data part of data register 9	BSI_D9_ DAT
BSI +0054h	Control part of data register 10	BSI_D10_CON
BSI +0058h	Data part of data register 10	BSI_D10_ DATA
BSI +005Ch	Control part of data register 11	BSI_D11_CON
BSI +0060h	Data part of data register 11	BSI_D11_ DAT
BSI +0064h	Control part of data register 12	BSI_D12_CON
BSI +0068h	Data part of data register 12	BSI_D12_ DAT
BSI +006Ch	Control part of data register 13	BSI_D13_CON

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BSI +0070h	Data part of data register 13	BSI_D13_ DAT
BSI +0074h	Control part of data register 14	BSI_D14_CON
BSI +0078h	Data part of data register 14	BSI_D14_ DAT
BSI +007Ch	Control part of data register 15	BSI_D15_CON
BSI +0080h	Data part of data register 15	BSI_D15_ DAT
BSI +0084h	Control part of data register 16	BSI_D16_CON
BSI +0088h	Data part of data register 16	BSI_D16_ DAT
BSI +008Ch	Control part of data register 17	BSI_D17_CON
BSI +0090h	Data part of data register 17	BSI_D17_ DAT
BSI +0094h	Control part of data register 18	BSI_D18_CON
BSI +0098h	Data part of data register 18	BSI_D18_ DAT
BSI +009Ch	Control part of data register 19	BSI_D19_CON
BSI +00A0h	Data part of data register 19	BSI_D19_ DAT
BSI +00A4h	Control part of data register 20	BSI_D20_CON
BSI +00A8h	Data part of data register 20	BSI_D20_ DAT
BSI +00ACh	Control part of data register 21	BSI_D21_CON
BSI +00B0h	Data part of data register 21	BSI_D21_ DAT

Table 31 BSI data registers

6.2 Base-band Parallel Interface

6.2.1 General description

The Base-band Parallel Interface is an 8-pin output bus used for timing-critical control of the external circuits. These pins are typically used to control front-end components at the specified time along the GSM time-base, such as transmit-enable, GSM/DCS/PCS band switching, TR-switch, … etc.

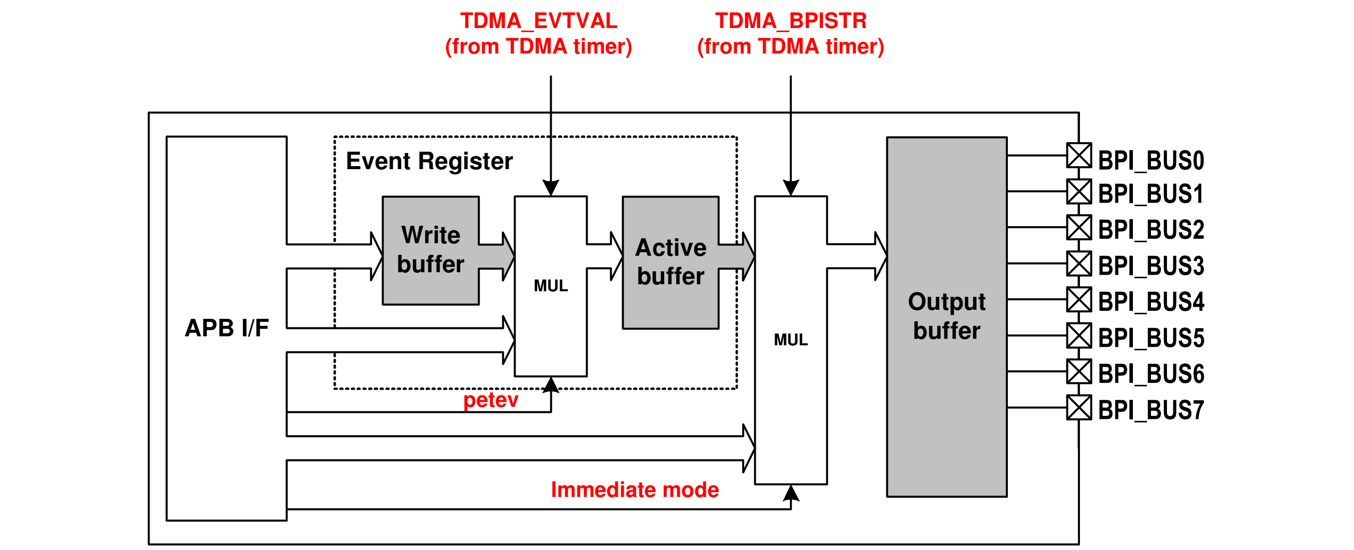

Figure 38 Block diagram of BPI interface

An 8-bit by 13 table is programmed by the MCU in order to define the output value of BPI_BUS0~BPI_BUS7. Each TDMA_BPI event triggers the transfer of the corresponding value in the table to the output buffer, thus change the value of the BPI bus. If any TDMA_BPI event is disabled in the TDMA timer, the corresponding signal TDMA_BPI will not be pulsed, and the corresponding transfer will not take place and the value on the BPI bus will remain unchanged.

The BPI data registers are double-buffered, the transfer from the write buffer to the active buffer takes place on the TDMA_EVTVAL signal, and the transfer from the active buffer to the output buffer takes place on TDMA_BPI events signaled by TDMA_BPI.

For applications in which BPI signals serve as the switch, typically some current-driving components are added to enhance the driving capability. We provide 3 configurable output pins with up to 8mA current. It's intended to reduce the number of the external components.

The output pin BPI_BUS7 is multiplexed with other functions. To enable it, the mode control field (GPIObase+24)[15:14] should be set to 01. Note that BSI_CS1 of the BSI and BPI_BUS7 couldn't be used at the same time.

6.2.2 Register Definitions

BPI+0000h BPI control register BPI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PINM2	PINM1	PINM0	PETEV
Type													WO	WO	WO	R/W
Reset													0	0	0	0

The register is the control register of the BPI unit. It controls the direct access mode of the active buffer and the current driving mode for the output pins.

The driving capability of BPI_BUS0, BPI_BUS1, and BPI_BUS2 can be 4mA or 8mA, selected by PINM0, PINM1, and PINM2, respectively. To provide high driving capability can save some external current-driving components. The driving capability of BPI_BUS3, BPI_BUS4, BPI_BUS5, BPI_BUS6, and BPI_BUS7 is 2mA.

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PETEV The flag is used to enable the direct access to the active buffer.

- **0** The MCU writes data to the write buffer. The data is latched in the active buffer after the TDMA_EVTVAL signal is pulsed.
- **1** The MCU directly writes data to the active buffer without waiting for the TDMA_EVTVAL signal.

PINM0 The field controls the driving capability of BPI_BUS0.

- **0** The output driving capability is 4mA.
- **1** The output driving capability is 8mA.

PINM1 The field controls the driving capability of BPI_BUS1.

- **0** The output driving capability is 4mA.
- **1** The output driving capability is 8mA.

PINM2 The field controls the driving capability of BPI_BUS2.

- **0** The output driving capability is 4mA.
- **1** The output driving capability is 8mA.

BPI +0004h BPI data register 0 BPI_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The register defines the signals of the 8 BPI output pins after the event TDMA_BPI0 takes place. There are 13 registers, which is associated with 13 events, of the same type as listed in **Table 32**. The data registers are all double-buffered. When PETEV is set to 0, the MCU writes to the write buffer. When PETEV is set to 1, the MCU writes to the active buffer.

POx The flag defines the corresponding value of the output pins BPIx after the event 0 takes place.

Register Address	Register Function	Acronym
BPI +0004h	BPI pin data for event TDMA_BPI0	BPI_DAT0
BPI +0008h	BPI pin data for event TDMA_BPI 1	BPI_DAT1
BPI +000Ch	BPI pin data for event TDMA_BPI 2	BPI_DAT2
BPI +0010h	BPI pin data for event TDMA_BPI 3	BPI_DAT3
BPI +0014h	BPI pin data for event TDMA_BPI 4	BPI_DAT4
BPI +0018h	BPI pin data for event TDMA_BPI 5	BPI_DAT5
BPI +001Ch	BPI pin data for event TDMA_BPI 6	BPI_DAT6
BPI +0020h	BPI pin data for event TDMA_BPI 7	BPI_DAT7
BPI +0024h	BPI pin data for event TDMA_BPI 8	BPI_DAT8
BPI +0028h	BPI pin data for event TDMA_BPI 9	BPI_DAT9
BPI +002Ch	BPI pin data for event TDMA_BPI 10	BPI_DATA
BPI +0030h	BPI pin data for event TDMA_BPI 11	BPI_DATB
BPI +0034h	BPI pin data for event TDMA_BPI 12	BPI_DATC
BPI +0038h	BPI pin data for immediate write	BPI_DATI

Table 32 BPI Data Registers

BPI +0060h BPI event enable register BPI_ENA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				BEN12	BEN11	BEN10	BEN9	BEN8	BEN7	BEN6	BEN5	BEN4	BEN3	BEN2	BEN1	BEN0
Type				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

The register is used to enable the events that are signaled by the TDMA timer. After hardware reset, all the enable bits are initialized as 1. Upon receiving the TDMA_EVTVAL pulse, those bits are also set to 1.

BENx The flag controls the function of event x.

- **0** The event x is disabled.
- **1** The event x is enabled.

6.3 Automatic Power Control (APC) Unit

6.3.1 General description

Automatic Power Control unit is used to control the Power Amplifier (PA). Through APC unit, we can set the proper transmit power level of the GSM handset and to ensure that the burst power ramping requirements are met. Two banks of ramp profiles can be provided in one TDMA frame. One is for ramp-up, while the other for ramp-down. Each bank of the ramp profile consists of 16 8-bit values. Those are further multiplied by a scaling factor, and interpolated into 32 10-bit values. The block diagram of the APC unit is shown in **Figure 39**. The APB bus interface is 32 bits width. It takes 4 write accesses for each bank of ramp profile.

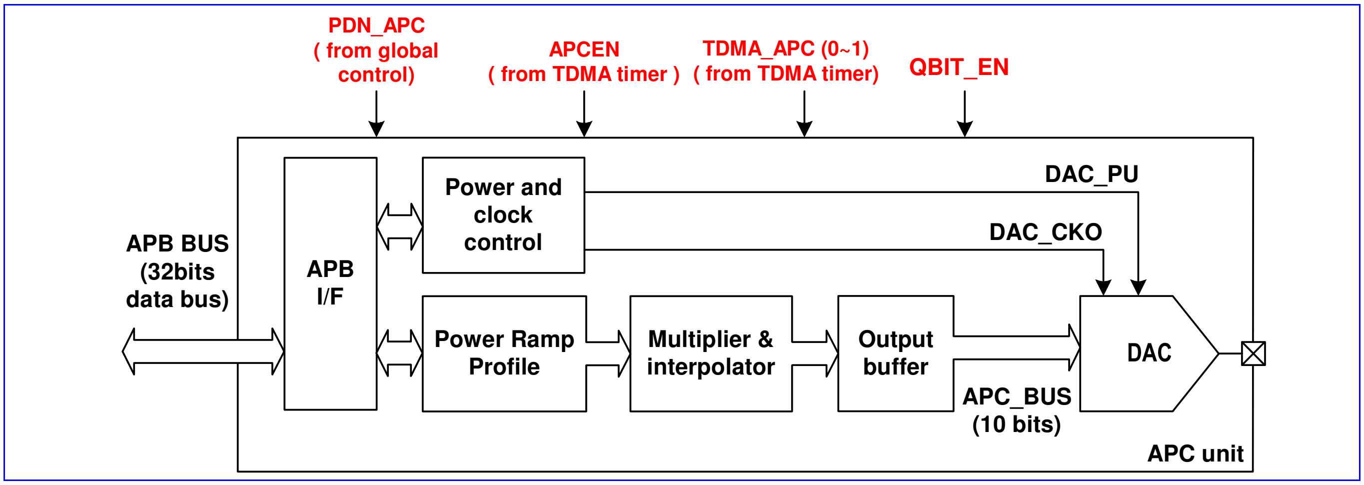

Figure 39 Block diagram of APC unit.

6.3.2 Register Definitions

APC+0000h Ramp up profile #0 APC_RAMPUP0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENT_UP3								ENT_UP2							
Type	R/W								R/W							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENT_UP1								ENT_UP0							
Type	R/W								R/W							

The register stores the first four entries of the power ramp-up profile. The first entry resides in the LSB byte [7:0], the second in the second byte [15:8], and so on. Since this register provides no hardware reset, the programmer should configure it before any APC event from the TDMA timer.

ENT_UP3 The 4th entry of the power ramp-up profile.
ENT_UP2 The 3rd entry of the power ramp-up profile.
ENT_UP1 The 2nd entry of the power ramp-up profile.
ENT_UP0 The 1st entry of the power ramp-up profile.

There are eight register of the same type listed as **Table 33**.

Register Address	Register Function	Acronym
APC +0000h	APC ramp up profile #0	APC_RAMPUP0
APC +0004h	APC ramp up profile #1	APC_RAMPUP1
APC +0008h	APC ramp up profile #2	APC_RAMPUP2
APC +000Ch	APC ramp up profile #3	APC_RAMPUP3
APC +0010h	APC ramp down profile #0	APC_RAMPDN0
APC +0014h	APC ramp down profile #1	APC_RAMPDN1
APC +0018h	APC ramp down profile #2	APC_RAMPDN2
APC +001Ch	APC ramp down profile #3	APC_RAMPDN3

Table 33 APC ramp up/down registers

APC+01C4h APC offset value APC_OFFSET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OFF									
Type							R/W									
Reset							0									

The register stores the pedestal value of the APC unit. The APC D/A converter is powered down when not transmitting. Right after the signal APC_EN has been asserted, the APC D/A converter is powered up and biased on the offset value stored in this register. It's intended to provide initial control voltage of the external control loop. We call it the pedestal value. The exact value depends on the characteristics of the external components.

OFF The field stores the pedestal value for the PA. After hardware reset, the value is 0.

APC+01C8h APC analog control APC_CALI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TEST	CALI				
Type											R/W	R/W				
Reset											0	0				

The register stores the calibration control values used for the analog part.

TEST The field signifies the buffer-bypass mode for the analog part. Set to be 1 enables it. It's recommended to be 0.
CALI The calibration values for the analog part.

APC +01CCh APC scaling factor APC_SCAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SCAL									

Type							R/W
Reset							1_0000_0000

The register stores the scaling factor. After hardware reset, the initial value of the register is 256. In that case, no scaling in done, that is, each entry of the ramp profile is multiplied by 1. That's because 8 least significant bits will be truncated after multiplication.

SCAL The field is the scaling factor. After hardware reset, the value is 256 by default.

6.3.3 Ramp profile programming

The first value of the normalized ramp-up profile should be written in the lowest byte of the RAMPUP0 register. The second value should be written in the second lowest byte of the RAMPUP0, and vice versa.

The start of ramping is triggered by the TDMA_APC0/1 signals. The timing relationship of TDMA_APC0/1 and TDMA slots is depicted in **Figure 40**. TDMA_APC0 is always used for triggering ramp-up process, while TDMA_APC1 is for ramp-down. The power ramping profile should adapt to the characteristics of the external circuit and conform the timing mask defined in GSM SPEC 05.05.

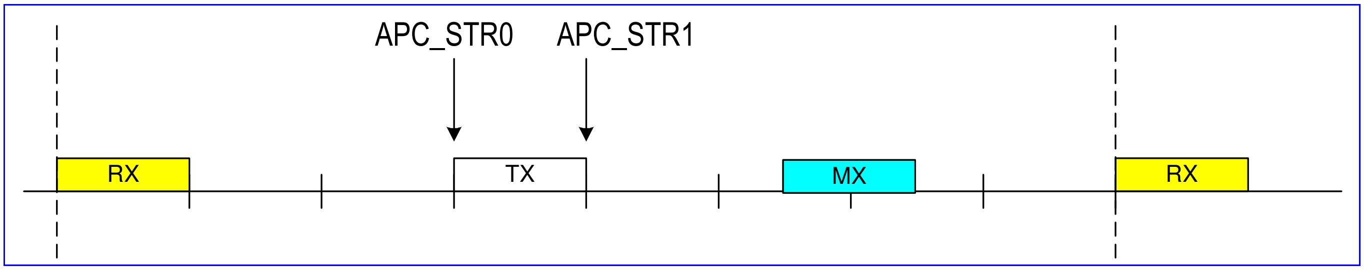

Figure 40 Timing diagram of TDMA_APC0 and TDMA_APC1

During each ramp process, each word of the normalized profile is first multiplied by a 10-bit scaling factor to form a bank of 18-bit words. The lowest 8-bit will be then punctured. The scaling factor is reset on hexadecimal 100. The value smaller than hexadecimal 100 will scale down the ramp profile, while the larger value will scale up the ramp profile.

The 16 10-bit words are interpolated into 32 10-bit words by the hardware. The interpolator calculates the average values between successive output values following the equations below:

$$APC_BUS_{2k} = APC_OFFSET + \frac{APC_DATA_{k-1} + APC_DATA_{k}}{2}$$

$$APC_BUS_{2k+1} = APC_OFFSET + APC_DATA_{k}$$

$$k = 0,1,...,15$$

A 10-bit D/A converter is then used to convert these 32 ramp values in a rate of 1.0833MHz. The timing diagram is shown in **Figure 41** and the output will be maintained on the final value A31 before the next event occurs.

The timing diagram of DAC_CLK and DAC_BUS in detail is as depicted in **Figure 42**. In practice, the period of QBIT_EN will be 12 times of the system clock, that is, 13/12 MHz. The period in the figure is only 6 times just for illustration. The data on DAC_OUT is further latched in the sample register of the D/A converter at the falling edge of DAC_CKO. The DAC_CKO pulse is only generated continuously in the window of APC_EN.

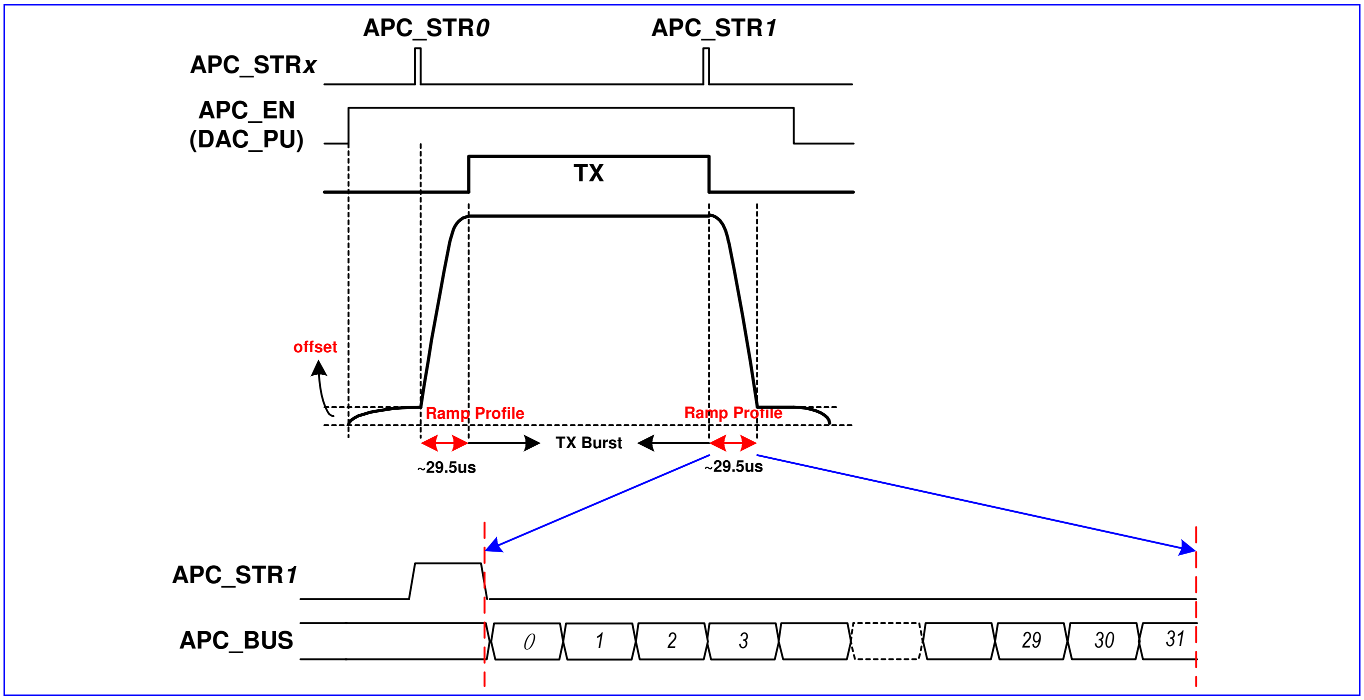

Figure 41 Timing diagram of the APC ramping.

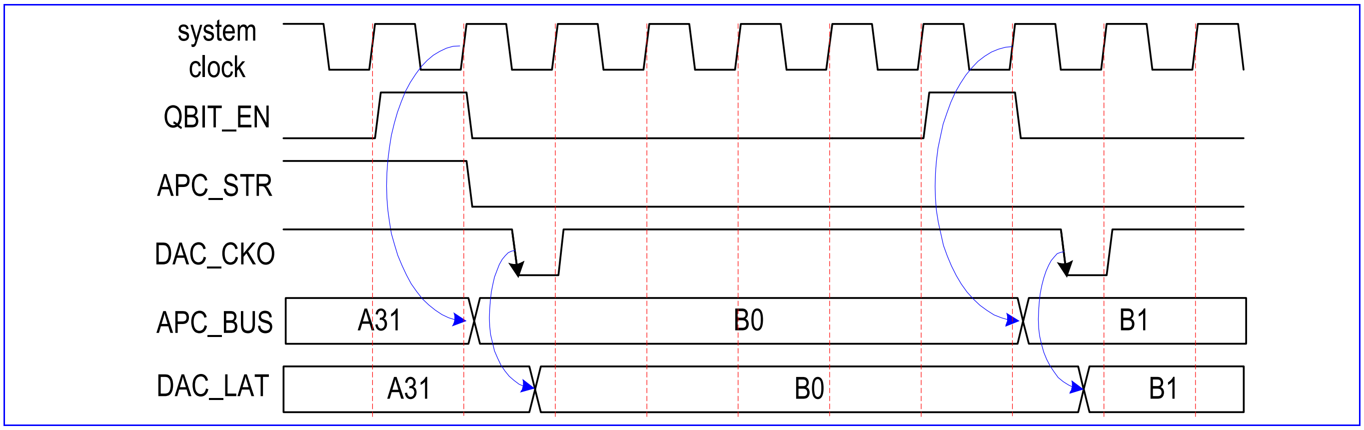

Figure 42 Timing diagram of interpolator in the APC unit

Since the profile is not double-buffered, the timing to write the ramping profile would be critical. The programmer should prevent from writing the data buffer about the time that the ramping process is taking place. Or it would interfere the current action and cause malfunction.

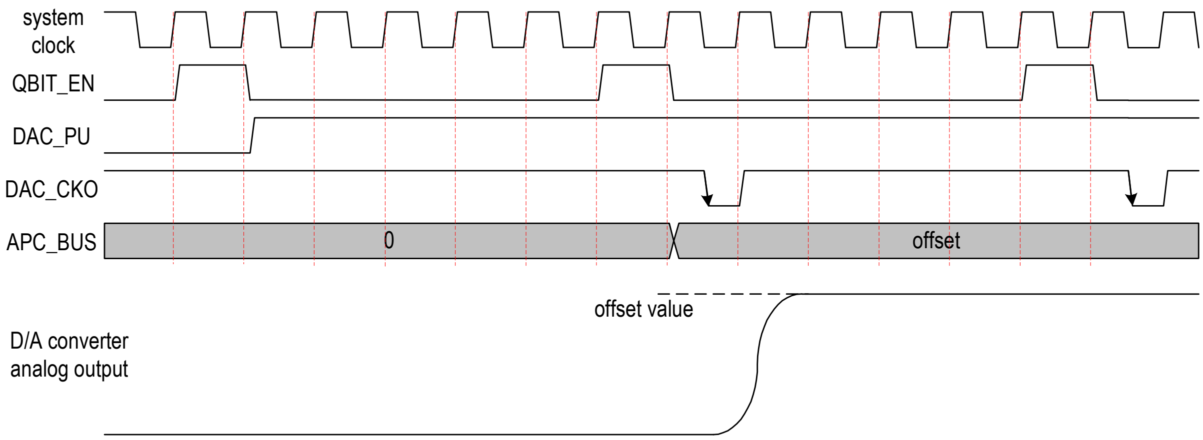

Figure 43 Timing diagram of initial offset in the APC unit

The signal DAC_PU controls the power on/off of the D/A converter. The timing in controlled by the signal APCEN from the TDMA timer. When APCEN is asserted, the D/A is activated and biased at a programmable offset value, further powers on the PA. It is used to provide the pedestal function for the PA. The timing diagram is depicted in **Figure 43**. The APC unit de-activates the D/A converter after APCEN is de-asserted. When the D/A converter is powered off, the analog output remains no driving.

6.4 Automatic Frequency Control (AFC) Unit

6.4.1 General description

Automatic Frequency Control unit provides the direct control of the oscillator for frequency offset and Doppler shift compensation. The block diagram is depicted in **Figure 44**. It utilizes a 13-bit D/A converter to achieve high-resolution control. Two modes of operation are supported and described as follows.

In timer-triggered mode, the TDMA timer controls the AFC enabling events. There provided at most four events within one TDMA frame. Double buffer architecture is supported. The AFC values can be written to the write buffers. When the event validate signal takes place, the values in the write buffers will be latched in the active buffers. The AFC values can also be written to the active buffers directly. When an indexed AFC event takes place, the value in the corresponding active buffer with the same index take effect. The timing diagram of AFC events in terms of TX/RX/MX windows is depicted in **Figure 45**. In this mode, the D/A converter can be either powered on continuously or for a programmable duration (of 256 quarter-bits by default). The later option is for power saving.

In immediate mode, the MCU can directly control the AFC value without event triggering. The value written by the MCU immediately takes effect. In this mode, the D/A converter should be powered on continuously. When entering timer-triggered mode from immediate mode, the D/A converter will be kept powered on for a programmable duration (of 256 quarter-bits by default) if the next TDMA_AFC has been not pulsed in the duration. The duration will be prolonged upon receiving next events.

The two modes provide flexibility when controlling the oscillator. The 13-bit DAC proves to be monotonic. Associated with proper AFC algorithm, MT6205B achieves good tracking of the RF channels and the highest performance.

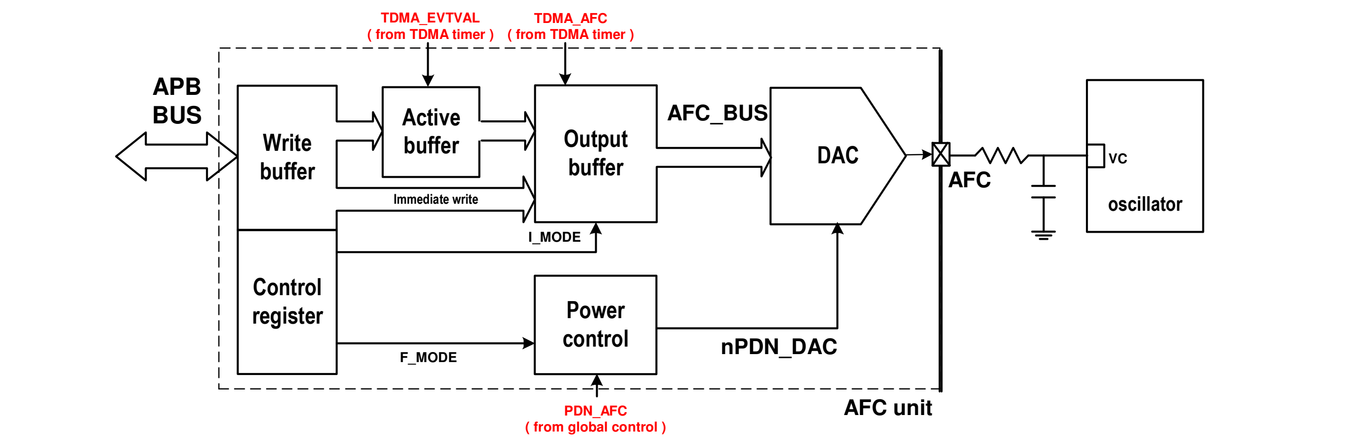

Figure 44 The block diagram of the AFC controller

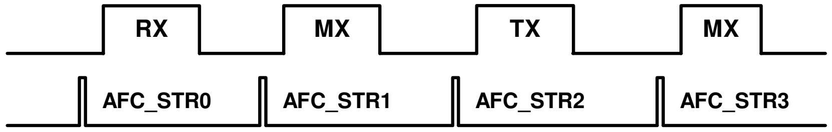

Figure 45 The timing diagram of the AFC controller

6.4.2 Register Definitions

AFC+0000h AFC control register AFC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RDACT	F_MODE	FETENV	I_MODE
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

Four control modes are defined and can be controlled through the AFC control register AFC_CON. F_MODE enables the force power up mode. FETENV enables the directly writing operation to the active buffer. I_MODE enables the immediate mode. RDACT enables the directly reading operation from the active buffer.

RDACT The flag enables the directly reading operation from the active buffer. Note the control flag is only applicable to the double buffer.

0 APB read from the write buffer.

1 APB read from the active buffer.

FETENV The flag enables the directly writing operation to the active buffer. Note the control flag is only applicable to the double buffer.

0 APB write to the write buffer.

1 APB write to the active buffer.

F_MODE The flag enables the force power up mode.

0 The force power up mode is not enabled.

1 The force power up mode is enabled.

I_MODE The flag enables the immediate mode.

0 The immediate mode is not enabled.

1 The immediate mode is enabled.

AFC +0004h AFC data register 0 AFC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AFCD												
Type				R/W												

The register stores the AFC value for the event 0 triggered by the TDMA timer in timer-triggered mode. When RDACT or FETENV is set, the data transfer operates on the active buffer. Contrarily, when RDACT or FETENV is not set, the data transfer operates on the write buffer.

There are four registers (AFC_DAT0, AFC_DAT1, AFC_DAT2, AFC_DAT3) of the same type, which for each corresponds to the event triggered by the TDMA timer. AFC_DAT0 is particularly used for the immediate mode. In this mode, only the value is the AFC_DAT0 write buffer is used to control the D/A converter. The four registers are summarized in **Table 34**.

The registers have no initial values. So it has to be programmed before any AFC event takes place. However, the AFC value for the D/A converter, i.e., the output buffer value, is initially 0 right after power up before any event takes place.

AFCD The field is the AFC sample for the D/A converter.

Register Address	Register Function	Acronym
AFC +0004h	AFC control value 0	AFC_DAT0
AFC +0008h	AFC control value 1	AFC_DAT1
AFC +000Ch	AFC control value 2	AFC_DAT2
AFC +0010h	AFC control value 3	AFC_DAT3

Table 34 AFC Data Registers

AFC +0014h AFC power up period AFC_PUPER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PU_PER												
Type				R/W												
Reset				ff												

The register stores the AFC power up period, which is 13 bits width. The value ranges from 0 to 8191. If the flag F_MODE is set, this register has no effect since the D/A converter is powered up continuously. If the flag F_MODE is not set, this register takes control of the power up duration of the D/A converter. After triggered by the TDMA timer, the signal nPDN_DAC as shown in **Figure 44** will be set to be 1 to power up the D/A converter and not be reset to be 0 until the counter expires.

PU_PER The field signifies the AFC power up period. After hardware power up, the field is initialized as 255.

AFC +001Ch AFC analog control AFC_CALI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TEST		CHPUMP	RSDON	CALI				
Type								R/W		R/W	R/W	R/W				
Reset								0		0	0	0				

The register stores the control flags for the analog part.

TEST For test purpose only.

CHPUMP The field controls the charge pump circuit in the analog part. It's recommended to be 0.

RSDON For test purpose only.

CALI The field signifies the calibration control values, which control the bias current of the analog part.

7 Baseband Front End

Baseband Front End is a modem interface between GSM TX/RX mixed-signal modules and digital signal processor (DSP). We can divide this block into two parts (see **Figure 46**). The first is the uplink (transmitting) path, which converts bit-stream from DSP into digital in-phase (I) and quadrature (Q) signals for GSM TX mixed-signal module. The second part is the downlink (receiving) path, which receives digital in-phase (I) and quadrature (Q) signals from GSM RX mixed-signal module, performs FIR filtering and then sends results to DSP. **Figure 46** illustrates interconnection around Baseband Front End. In the figure the shadowed blocks compose Baseband Front End. The uplink path is mainly composed of GMSK Modulator and uplink parts of Baseband Port, and the downlink path is mainly composed of RX digital FIR filter and downlink parts of Baseband Port. Baseband Port is a interface used to communicate with DSP. In addition, there is a set of control registers in Baseband Front End that is intended for control of GSM TX/RX mixed-signal modules, inclusive of calibration of DC offset and gain mismatch of downlink analog-to-digital (A/D) converters as well as uplink digital-to-analog (D/A) converters in GSM TX/RX mixed-signal modules. The timing of bit streaming through Baseband Front End is completely under control of TDMA timer. Usually only either of uplink and downlink paths is active at one moment. However, both of the uplink and downlink paths will be active simultaneously when Baseband Front End is in loopback mode.

When either of TX windows in TDMA timer is opened, the uplink path in Baseband Front End will be activated. Accordingly components on the uplink path such as GMSK Modulator will be powered on, and then GSM TX mixed-signal module is also powered on. The subblock Baseband Port will sink TX data bits from DSP and then forward them to GMSK Modulator. The outputs from GMSK Modulator are sent to GSM TX mixed-signal module. Finally D/A conversions are performed in GSM TX mixed-signal module and the output analog signal is output to RF module.

Similarly, while either of RX windows in TDMA timer is opened, the downlink path in Baseband Front End will be activated. Accordingly components on the downlink path such as GSM RX mixed-signal module and RX digital FIR filter are then powered on. First A/D conversions are performed in GSM RX mixed-signal module, and then the results are sourced to RX digital FIR filter. Low-Pass filtering is performed in RX digital FIR filter. Finally the results will be sourced to DSP through Baseband Port.

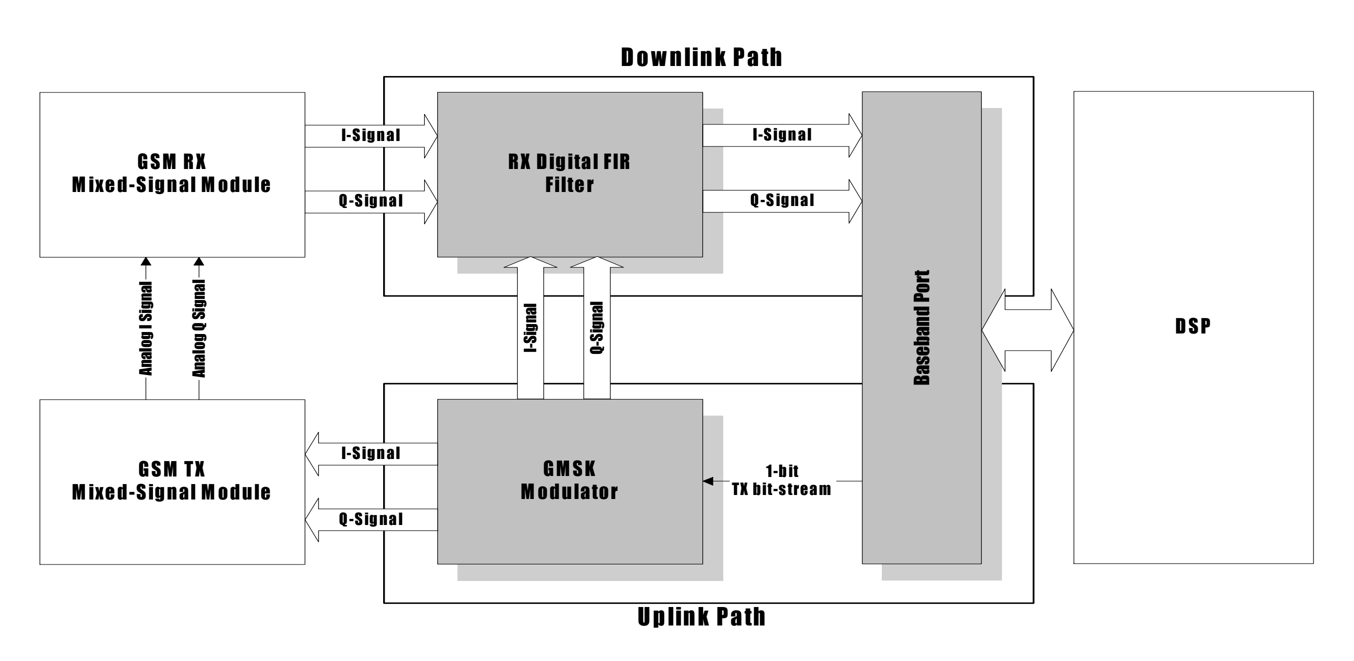

Figure 46 Block Diagram Of Baseband Front End

7.1 Baseband Port

7.1.1 General Description

Baseband Front End communicates with DSP through the sub block of Baseband Port. It implies that DSP must be configured carefully in order to have Baseband Port cooperate with DSP core correctly.

If downlink path is programmed in bypass-filter mode (**NOT** bypass-filter loopback mode), behavior of Baseband Port will completely be different from that in normal function mode. The special mode is for testing purpose. Please see the subsequent section of Downlink Path for details.

TX and RX windows are under control of TDMA timer. Please refer to functional specification of TDMA timer for the details how to open/close a TX/RX window. Opening/Closing of TX/RX windows has two major effects on Baseband Front End. They are power on/off of corresponding components and data souring/sinking. It is worth noticing that Baseband Port is only intended for sinking TX data from DSP or sourcing data to DSP. It does not involve power on/off of GSM TX/RX mixed-signal modules.

As far as downlink path is concerned, if a RX window is opened by TDMA timer Baseband Front End will have GSM RX mixed-signal module proceed to make A/D conversion, RX digital filter proceed to perform filtering and Baseband Port be activated to source data from RX digital filter to DSP no matter the data is meaningful or not. However, the interval between the moment that GSM RX mixed-signal module is powered on and the moment that data proceed to be dumped by Baseband Port can be well controlled in TDMA timer. Lets denote as RX enable window the interval that GSM RX mixed-signal module is powered on and denote as RX dump window the interval that data is dumped by Baseband Port. If the first samples from RX digital filter desire to be discarded, the corresponding RX enable window must cover the corresponding RX dump window. Notes that RX dump windows always win over RX enable windows. It means that a RX

dump window will always raise a RX enable window. RX enable windows can be raised by TDMA timer or by programming RX power-down bit in global control registers to be ‘0’. It is useful in debugging environment.

Similarly, a TX dump window refers to the interval that Baseband Port sinks data from DSP on uplink path and a TX enable window refers to the interval that GSM TX mixed-signal module is powered on. A TX window controlled by TDMA timer involves a TX dump window and a TX enable window simultaneously. The interval between the moment that GSM TX mixed-signal module is powered on and the moment that data proceed to be forwarded from DSP to GMSK modulator by Baseband Port can be well controlled in TDMA timer. TX dump windows always win over TX enable windows. It means that a TX dump window will always raise a TX enable window. TX enable windows can be raised by TDMA timer or by programming TX power-down bit in global control registers to be ‘0’. It is useful in debugging environment.

Accordingly, Baseband Port are only under control of TX/RX dump window. Note that if TX/RX dump window is not integer multiples of bit-time it will be extended to be integer multiples of bit-time. For example, if TX/RX dump window has interval of 156.25 bit-times then it will be extended as 157 bit-times in Baseband Port.

7.1.2 Register Definitions

BFE+00D0h Base-band Common Control Register BFE_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BCIEN
Type																R/W
Reset																0

This register is for common control of Baseband Front End. It consists of ciphering encryption control.

BCIEN The bit is for ciphering encryption control. If the bit is set to ‘1’, XOR will performed on some TX bits (payload of Normal Burst) and ciphering pattern bit from DSP, and then the result is forwarded to GMSK Modulator. Meanwhile, Baseband Front End will generate signals to drive DSP ciphering process produce corresponding ciphering pattern bits if the bit is set to ‘1’. If the bit is set to ‘0’, the TX bit from DSP will be forwarded to GMSK modulator directly. Baseband Front End will not activate DSP ciphering process.

0 Disable ciphering encryption.

1 Enable ciphering encryption.

BFE +00D4h Base-band Common Status Register BFE_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BULFS	BULEN	BDLFS	BDLEN
Type													RO	RO	RO	RO
Reset													0	0	0	0

This register indicates status of Baseband Front End. Under control of TDMA timer, Baseband Front End can be driven in several statuses. If downlink path is enabled, then the bit BDLEN will be ‘1’. Otherwise the bit BDLEN will be ‘0’. If downlink parts of Baseband Port is enabled, the bit BDLFS will be ‘1’. Otherwise the bit BDLFS will be ‘0’. If uplink path is enabled, then the bit BULEN will be ‘1’. Otherwise the bit BULEN will be 0. If uplink parts of Baseband Port is enabled, the bit BULFS will be ‘1’. Otherwise the bit BULFS will be ‘0’. Once downlink path is enabled, GSM RX mixed-signal module will also be powered on. Similarly, once uplink path is enabled, GSM TX mixed-signal module will also be powered on. Furthermore, enabling Baseband Port for downlink path refers to dumping results from RX digital FIR filter to DSP. Similarly, enabling Baseband Port for uplink path refers to forwarding TX bit from DSP to GMSK modulator.

BDLEN stands for "**B**aseband **D**own**L**ink **EN**able". BULEN stands for "**B**aseband **U**p**L**ink **EN**able". BDLFS stands for "**B**aseband **D**own**L**ink **F**rame**S**ync". BULFS stands for "**B**aseband **U**p**L**ink **F**rame**S**ync".

BDLEN Indicate if downlink path is enabled.

- **0** Disabled
- **1** Enabled

BDLFS Indicate if Baseband Port for downlink path is enabled.

- **0** Disabled
- **1** Enabled

BULEN Indicate if uplink path is enabled.

- **0** Disabled
- **1** Enabled

BULFS Indicate if Baseband Port for uplink path is enabled.

- **0** Disabled
- **1** Enabled

7.2 Downlink Path (RX Path)

7.2.1 General Description

On downlink path, the subblock between GSM RX mixed-signal module and Baseband Port is RX Path. It mainly consists of a digital FIR filter, two sets of multiplexing paths for loopback modes, interface for GSM RX mixed-signal module and interface for Baseband Port. The block diagram is shown in **Figure 47**.

While RX enable windows are opened, RX Path will issue control signals to have GSM RX mixed-signal module proceed to make A/D conversion. As each conversion is finished, one set of I/Q signals will be latched. There exists a digital FIR filter for these I/Q signals. The result of filtering will be dumped to Baseband Port whenever RX dump windows are opened.

In addition to normal function, there are two loopback modes in RX Path. One is bypass-filter loopback mode, and the other is through-filter loopback mode. They are intended for verification of DSP firmware and hardware. The bypass-filter loopback mode refers to that RX digital FIR filter is not on the loopback path. However, the through-filter loopback mode refers to that RX digital FIR filter is on the loopback path.

The I/Q swap functionality is used to swap I/Q channel signals from GSM RX mixed-signal module before they are latched into RX digital FIR filter. It is intended to provide flexibility for I/Q connection with RF modules.

There is a special data path not shown in **Figure 47**. It is a data path from GSM RX mixed-signal module to Baseband Port. If downlink path is programmed in "Bypass RX digital FIR filter" mode, ADC outputs out of GSM RX mixed-signal module will be directed into Baseband Port directly. Therefore these data can be dumped into DSP and RX FIR filtering will not be performed on them. Limited by bandwidth of the serial interface between Baseband Port and DSP, only ADC outputs which are from either I-channel or Q-channel ADC can be dumped into DSP. Both of I- and Q-channel ADC outputs cannot be dumped simultaneously. Which channel will be dumped is controlled by the register bit SWAP of the register **RX_CFG** when downlink path is programmed in "Bypass RX digital FIR filter" mode. See register definition below for details. The mode is for measurement of performance of A/D converters in GSM RX mixed-signal module.

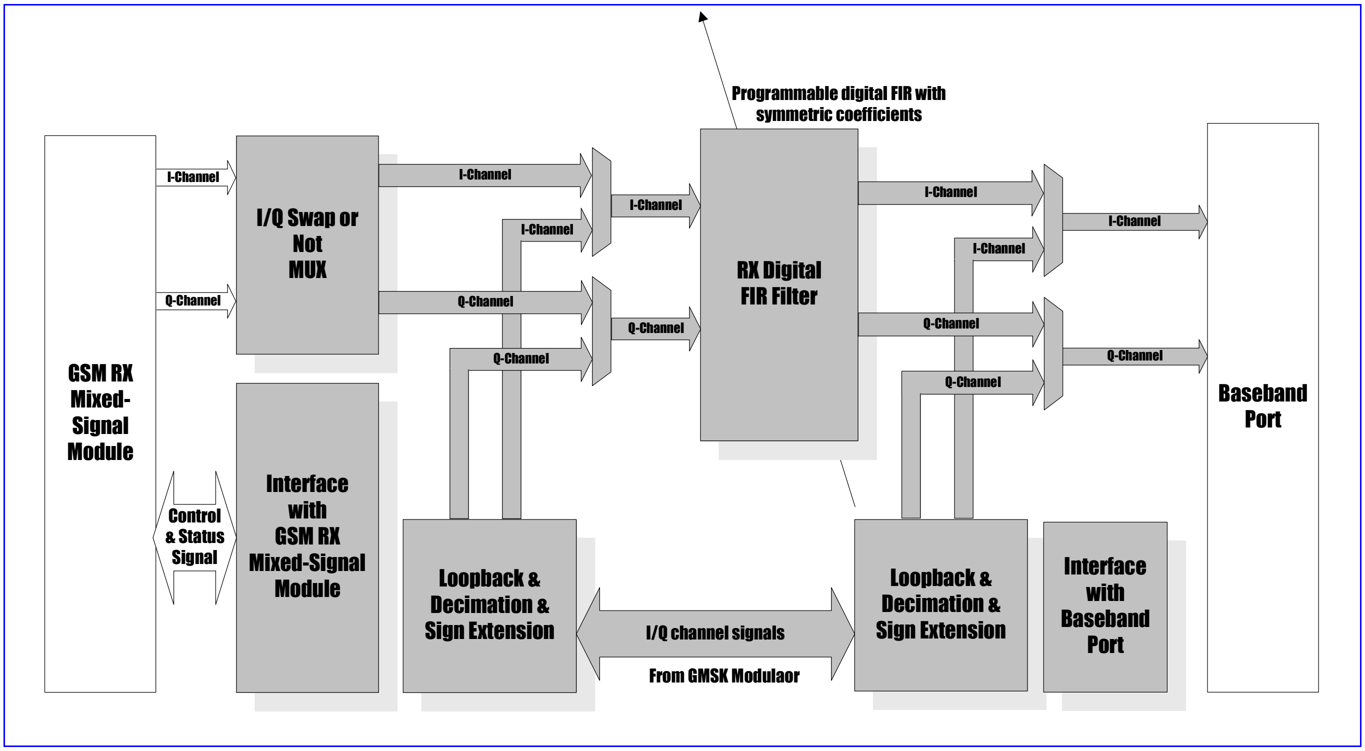

Figure 47 Block Diagram Of RX Path

7.2.2 Register Definitions

BFE +0000h RX Configuration Register RX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BYPF LTR	GAIN	QLPSEL[1:0]		ILPSEL[1:0]		OFFC AL	CHOP	SWAP	
Type							R/W	R/W	R/W		R/W		R/W	R/W	R/W	
Reset							0	0	00		00		0	0	0	

This register is for configuration of downlink path, inclusive of configuration of GSM RX mixed-signal module and RX path in Baseband Front End.

SWAP The register bit is for control of whether I/Q channel signals need swap before they are input to Baseband Front End. It provides flexibility of connection of I/Q channel signals between RF module and baseband module. The register bit has another purpose when the register bit "BYPFLTR" is set to 1. Please see description for the register bit "BYPFLTR".

0 I- and Q-channel signals are not swapped

1 I- and Q-channel signals are swapped

CHOP The register bit is used to determine if chopping mechanism in GSM RX mixed-signal module is applied.

0 Chopping is disabled

1 Chopping is enabled

OFFCAL The register bit is used to configure GSM RX mixed-signal module in a specific state for RF offset calibration.

0 Configure GSM RX mixed-signal module not in the state for RF offset calibration

1 Configure GSM RX mixed-signal module in the state for RF offset calibration

ILPSEL Loopback configuration selection for I-channel in GSM RX mixed-signal module

00 Normal mode

01 Loopback TX analog I

10 Loopback TX analog Q

11 Select the grounded input

QLPSEL Loopback configuration selection for Q-channel in GSM RX mixed-signal module

00 Normal mode

01 Loopback TX analog Q

10 Loopback TX analog I

11 Select the grounded input

Loopback configuration selection in GSM RX mixed-signal module is shown in **Figure 48**.

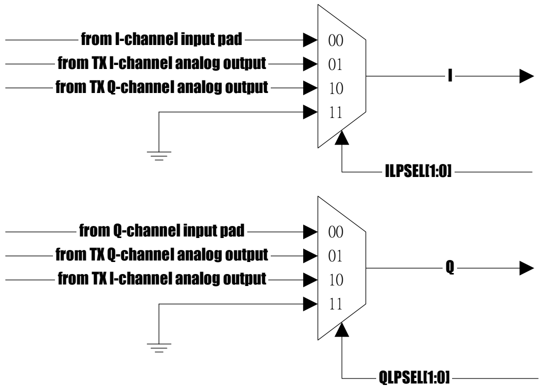

Figure 48 Loopback configuration selection in GSM RX mixed-signal module

GAIN The register bit is for configuration of the full swing input range of GSM RX mixed-signal module.

0 RX mixed-signal module's full swing input range = 0.8 * AVDD.

1 RX mixed-signal module's full swing input range = 0.4 * AVDD.

BYPFLTR Bypass RX FIR filter control. The register bit is used to configure Baseband Front End in the state called "Bypass RX FIR filter state" or not. Once the bit is set to '1', RX FIR filter will be bypassed. That is, ADC outputs of GSM RX mixed-signal module that are 11-bit resolution and at sampling rate of 1.083MHz can be dumped into DSP by Baseband Port and RX FIR filtering will not be performed on them. Limited by bandwidth of the serial interface between Baseband Port and DSP, these ADC outputs are all from either I-channel or Q-channel ADC. Both of I- and Q-channel ADC outputs cannot be dumped simultaneously. When the bit is set to '1' and the register bit "SWAP" is set to '0', ADC outputs of I-channel will be dumped. When the bit is set to '1' and the register bit "SWAP" is set to '1', ADC outputs of Q-channel will be dumped.

0 Not bypass RX FIR filter

1 Bypass RX FIR filter

BFE +0004h RX Threshold Register RX_THD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RXTHD										
Type						R/W										
Reset						01111111111										

This register is used to set threshold value of RX ADC outputs. If the value of RX ADC outputs is larger than or equal to the value defined in the register, then clipping of RX ADC outputs takes place. If it takes place on I-channel RX ADC outputs, then the value of the register RX_IOVF will increment. Similarly, if on Q-channel then the value of the register RX_QOVF will increment.

RXTHD Threshold value of RX ADC outputs. The value is coded in 2's complement, that is, has maximum value of 1023 and minimum value of –1024.

BFE +0008h RX I-Channel Overflow Status Register RX_IOVF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IOVF									
Type							R									

This register shows the status of clipping of I-channel RX ADC outputs. Notes that the value is updated only when 600 samples from I-channel RX ADC are received. That is, the result of clipping detection is valid when 600 samples from I-channel RX ADC are received.

IOVF Status of clipping of I-channel RX ADC outputs.

BFE +000Ch RX Q-Channel Overflow Status Register RX_QOVF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							QOVF									
Type							R									

This register shows the status of clipping of Q-channel RX ADC outputs. Notes that the value is updated only when 600 samples from Q-channel RX ADC are received. That is, the result of clipping detection is valid when 600 samples from Q-channel RX ADC are received.

QOVF Status of clipping of Q-channel RX ADC outputs.

BFE +0030h RX Control Register RX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BLPEN[1:0]		CALBIAS[4:0]				
Type										R/W		R/W				
Reset										0		00000				

This register is for control of downlink path, inclusive of control of GSM RX mixed-signal module and RX path in Baseband Front End module.

CALBIAS The register field is for control of biasing current in GSM RX mixed-signal module. It is coded in 2's complement. That is, its maximum is 15 and minimum is –16. Biasing current in GSM RX mixed-signal module has impact on performance of A/D conversion. Larger the value of the register field, larger is the biasing current in GSM RX mixed-signal module.

BLPEN The register field is for loopback configuration selection in Baseband Front End.

- **00** Configure Baseband Front End in normal function mode
- **01** Configure Baseband Front End in bypass-filter loopback mode
- **10** Configure Baseband Front End in through-filter loopback mode
- **11** Reserved

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BFE +0040h RX Digital FIR Filter Coefficient Register 0 RX_FIR_COEF0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 0. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256. It will be applied on the latest and the oldest taps of 31 taps. The equivalent process flow of RX digital FIR filtering is shown in **Figure 49**.

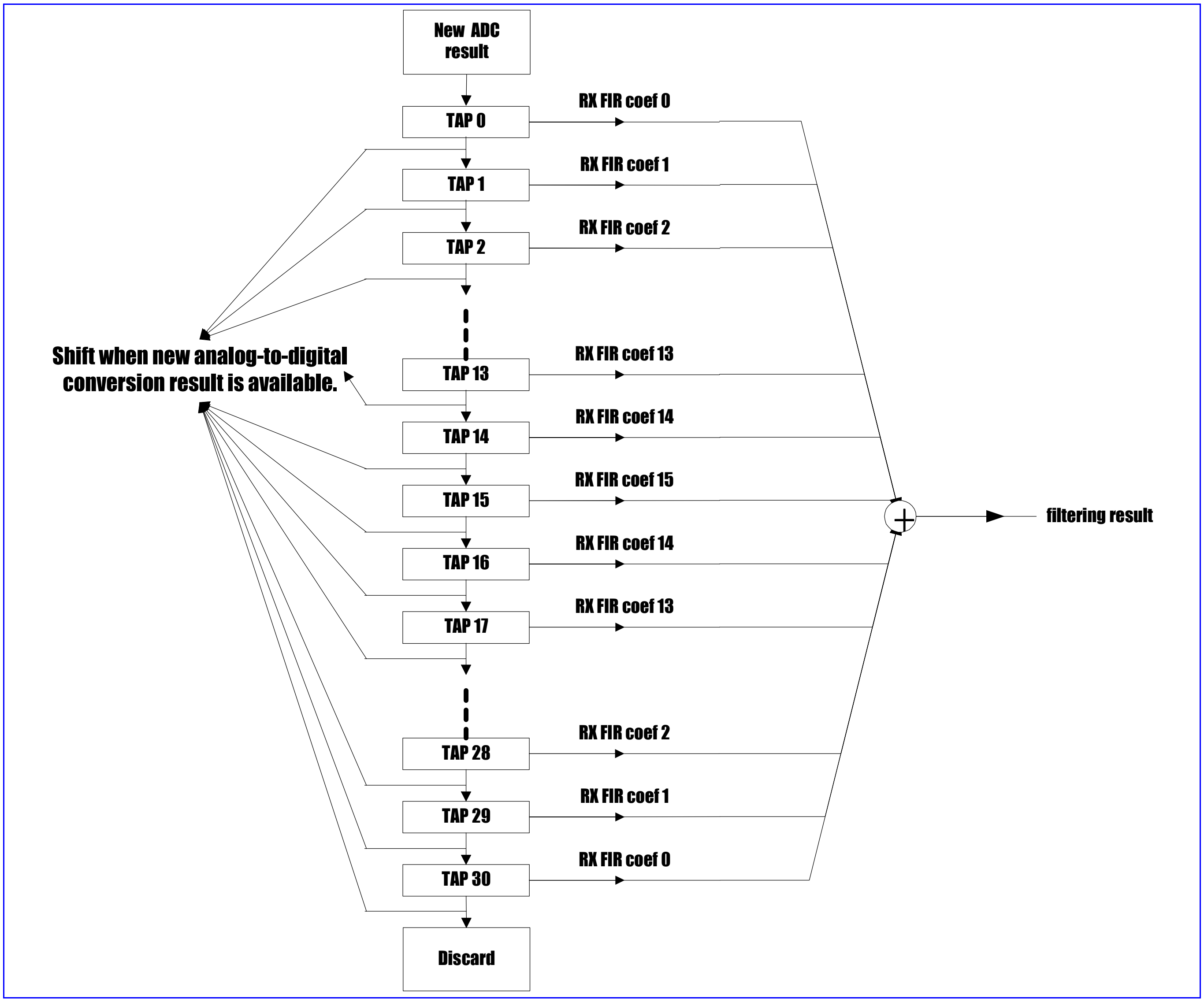

Figure 49 Equivalent Process Flow Of RX Digital FIR Filtering

BFE +0044h RX Digital FIR Filter Coefficient Register 1 RX_FIR_COEF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 1. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0048h RX Digital FIR Filter Coefficient Register 2 RX_FIR_COEF2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 2. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +004Ch RX Digital FIR Filter Coefficient Register 3 RX_FIR_COEF3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 3. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0050h RX Digital FIR Filter Coefficient Register 4 RX_FIR_COEF4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX FIR filter coefficient 4. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0054h RX Digital FIR Filter Coefficient Register 5 RX_FIR_COEF5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 5. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0058h RX Digital FIR Filter Coefficient Register 6 RX_FIR_COEF6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 6. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

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BFE +005Ch RX Digital FIR Filter Coefficient Register 7 RX_FIR_COEF7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 7. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0060h RX Digital FIR Filter Coefficient Register 8 RX_FIR_COEF8

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 8. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0064h RX Digital FIR Filter Coefficient Register 9 RX_FIR_COEF9

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 9. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0068h RX Digital FIR Filter Coefficient Register 10 RX_FIR_COEF10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 10. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +006Ch RX Digital FIR Filter Coefficient Register 11 RX_FIR_COEF11

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 11. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0070h RX Digital FIR Filter Coefficient Register 12 RX_FIR_COEF12

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 12. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0074h RX Digital FIR Filter Coefficient Register 13 RX_FIR_COEF13

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 13. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +0078h RX Digital FIR Filter Coefficient Register 14 RX_FIR_COEF14

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 14. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

BFE +007Ch RX Digital FIR Filter Coefficient Register 15 RX_FIR_COEF15

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is for RX digital FIR filter coefficient 15. It is coded in 2's complement. That is, its maximum is 255 and its minimum is –256.

7.3 Uplink Path (TX Path)

7.3.1 General Description

The purpose of the uplink path inside Baseband Front End is to sink TX symbols, one bit for each symbol, from DSP, then perform GMSK modulation on them, then perform offset cancellation on I/Q digital signals out of GMSK modulator, and finally control GSM TX mixed-signal module to make D/A conversion on I/Q signals out of GMSK Modulator with offset cancellation. Accordingly, the uplink path is composed of uplink parts of Baseband Port, GSM Encryptor, GMSK Modulator and Offset Cancellation. The block diagram of uplink path is shown in **Figure 50**. On uplink path, the content of a burst, including tail bits, data bits, and training sequence bits is sent from DSP. Translated by GMSK Modulator, these bits will become I/Q digital signals. Offset cancellation will be performed on these I/Q digital signals to compensate offset error of D/A converters (DAC) in GSM TX mixed-signal module. Finally the generated I/Q digital signals will be input to GSM

TX mixed-signal module that contains two DAC for I/Q signal respectively. The details of each subblock will be described in subsequent sections.

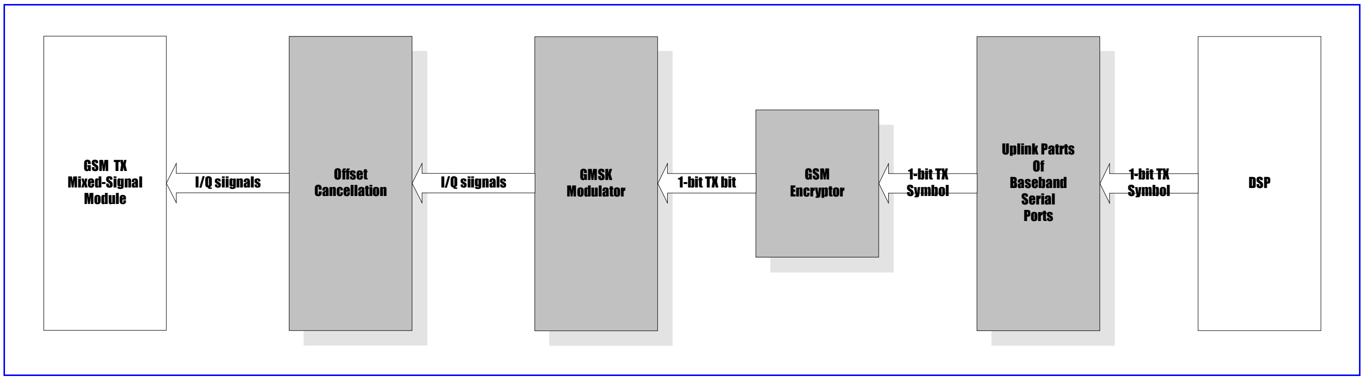

Figure 50 Block Diagram Of Uplink Path

TDMA timer having a quarter-bit timing accuracy gives the timing windows for uplink operation. Uplink operation is controlled by TX enable window and TX dump window of TDMA timer. Usually TX enable window is opened earlier than TX dump window. When TX enable window of TDMA timer is opened, uplink path in Baseband Front End will power on GSK TX mixed-signal module and thus has it drive valid outputs to RF module. However, uplink parts of Baseband Port still don't sink data from DSP through the interface between Baseband Port and DSP until now. Uplink parts of Baseband Port will not sink data from DSP until TX dump window of TDMA timer is opened.

7.3.2 Register Definitions

BFE +0010h TX Configuration Register TX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRIMQ[3:0]				TRIMI[3:0]				APNDEN	FLOAT	GAIN[2:0]			CMV[2:0]		
Type	R/W				R/W				R/W	R/W	R/W			R/W		
Reset	0000				0000				0	0	000			000		

This register is for configuration of uplink path, inclusive of configuration of GSM TX mixed-signal module and TX path in Baseband Front End.

CMV The register field is used to control common voltage in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 3 and minimum –4.

GAIN The register field is used to control gain of DAC in GSM TX mixed-signal module. It has impact on both of I- and Q-channel DAC in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 3 and minimum –4.

FLOAT The register field is used to have the outputs of DAC in GSM TX mixed-signal module float or not.

APNDEN Appending Bits Enable. The register bit is used to control the ending scheme of GMSK modulation.

- **0** Suitable for GPRS. If a TX enable window contains several TX dump window, then GMSK modulator will still output in the intervals between two TX dump window and all 1's will be fed into GMSK modulator during the intervals. **Note that when the bit is set to '0', the interval between the moment at which TX enable window is activated and the moment at which TX dump window is activated must be multiples of one bit time.**
- **1** Suitable for GSM only. After a TX dump window, GMSK modulator will only output for some bit times.

TRIMI The register field is used to control gain trimming of I-channel DAC in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 15 and minimum –16.

TRIMQ The register field is used to control gain trimming of Q-channel DAC in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 15 and minimum –16.

BFE +0014h TX I Channel Offset Compensation Register TX_OFFI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											OFFI[5:0]					
Type											R/W					
Reset											000000					

The register is for offset cancellation of I-channel DAC in GSM TX mixed-signal module. It is for compensation of offset error caused by I-channel DAC in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 31 and minimum –32.

OFFI Value of offset cancellation for I-channel DAC in GSM TX mixed-signal module

BFE +0018h TX Q Channel Offset Compensation Register TX_OFFQ

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											OFFQ[5:0]					
Type											R/W					
Reset											000000					

The register is for offset cancellation of Q-channel DAC in GSM TX mixed-signal module. It is for compensation of offset error caused by Q-channel DAC in GSM TX mixed-signal module. It is coded in 2's complement, that is, with maximum 31 and minimum –32.

OFFQ Value of offset cancellation for Q-channel DAC in GSM TX mixed-signal module

BFE +00C0h TX Control Register TX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALRCCNT						IQSWP	CALRC	CALRCSEL[2:0]			CALBIAS[4:0]				
Type	R/W						R/W	R/W	R/W			R/W				
Reset	10011						0	0	000			00000				

This register is for control of uplink path, inclusive of control of GSM TX mixed-signal module and TX path in Baseband Front End.

CALBIAS The register field is for control of biasing current in GSM TX mixed-signal module. It is coded in 2's complement. That is, its maximum is 15 and minimum is –16. Biasing current in GSM TX mixed-signal module has impact on performance of D/A conversion. Larger the value of the register field, larger is the biasing current in GSM TX mixed-signal module.

CALRCSEL The register field is for selection of cutoff frequency of smoothing filter in GSM TX mixed-signal module. It is coded in 2's complement. That is, its maximum is 3 and minimum is –4.

CALRC Whenever '1' is writing to the bit, calibration processing for smoothing filter in GSM TX mixed-signal module will be triggered. Once the calibration process is completed, the bit will be reset to 0 automatically.

IQSWP The register bit is for control of I/Q swapping. When the bit is set to '1', phase on I/Q plane will rotate in inverse direction.

0: I and Q are not swapped.

1: I and Q are swapped.

CALRCCNT Parameter for calibration processing of smoothing filter in GSM TX mixed-signal module. Default value is eleven. Note that it is **NOT** coded in 2's complement. Therefore the range of its value is from 0 to 15.

BFE +00C4h TX Calibration Result Register TX_CAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CALRCOUT[2:0]		
Type														R		

This register shows the result of calibration processing for smoothing filter in GSM TX mixed-signal module. Notes that the value becomes valid whenever the register bit CALRC in the register TX_CON return to '0' after writing '1' to it.

8 Timing Generator

Timing is the most critical issue in GSM applications. The TDMA timer provides a simple interface for the MCU to program all the timing-related events for receive event control, transmit event control and the timing adjustment. Detailed descriptions are seen in Section 8.1.

In pause mode, the 13MHz reference clock may be switched off temporarily for the purpose of power saving and the synchronization to the base-station is maintained by using a low power 32KHz crystal oscillator. The 32KHz oscillator is not accurate and therefore it should be calibrated prior to entering pause mode. The calibration sequence, pause begin sequence and the wake up sequence are described in Section 8.2.

8.1 TDMA timer

The TDMA timer unit is composed of three major blocks: Quarter bit counter, Signal generator and Event registers.

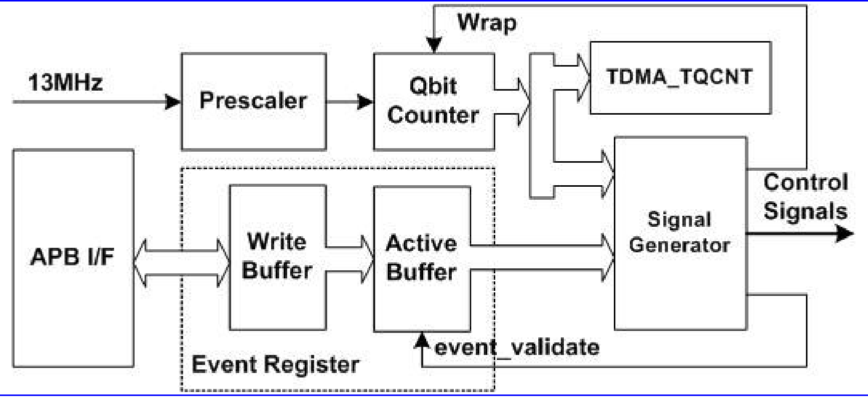

Figure 51 The block diagram of TDMA timer

By default, the quarter-bit counter continuously counts from 0 to the wrap position. In order to apply to cell synchronization and neighboring cell monitoring, the wrap position can be changed by the MCU to shorten or lengthen a TDMA frame. The wrap position is held in the TDMA_WRAP register and the current value of the TDMA quarter bit counter may be read by the MCU via the TDMA_TQCNT register.

The signal generator handles the overall comparing and event-generating processes. When a match is occurred between the quarter bit counter and the event register, a predefined control signal is generated. These control signals may be used for on-chip and off-chip purpose. Signals that change state more than once per frame make use of more than one event register.

The event registers are programmed to contain the quarter bit position of the event to be occurred. The event registers are double buffered. The MCU writes into the first register, and the event TDMA_EVTVAL transfers the data from the write buffer to the active buffer, which is used by the signal generator for comparison with the quarter bit count. The TDMA_EVTVAL signal itself may be programmed at any quarter bit position. These event registers could be classified into four groups:

On-chip Control Events

TDMA_EVTVAL
This event allows the data values written by the MCU to pass through to the active buffers.

TDMA_WRAP

TDMA quarter bit counter wrap position. This sets the position at which the TDMA quarter bit counter resets back to zero. The default value is 4999, changing this value will advance or retard the timing events in the frame following the next TDMA_EVTVAL signal.

TDMA_DTIRQ

DSP TDMA interrupt requests. DTIRQ triggers the DSP to read the command from the MCU/DSP Shard RAM to schedule the activities that will be executed in the current frame.

TDMA_CTIRQ1/CTIRQ2

MCU TDMA interrupt requests.

TDMA_AFC [3:0]

This signal powers up the automatic frequency control DAC for a programmed duration after this event.

Note: For both MCU and DSP TDMA interrupt requests, these signals are all active Low during one quarter bit duration and they should be used as edge sensitive events by the respective interrupt controllers.

On-chip Receive Events

TDMA_BDLON [3:0]

These registers are a set of four which contain the quarter bit event that initiates the receive window assertion sequence which powers up and enables the receive ADC, and then enables loading the receive data into the receive buffer.

TDMA_BDLOFF [3:0]

These registers are a set of four which contain the quarter bit event that initiates the receive window de-assertion sequence which disables loading the receive data into the receive buffer, and then powers down the receive ADC.

TDMA_RXWIN[3:0]

DSP TDMA interrupt requests. TDMA_RXWIN is usually used to initiate the related RX processing including two modes. In single-shot mode, TDMA_RXWIN is generated when the BRXFS signal is de-asserted. In repetitive mode, TDMA_RXWIN will be generated both regularly with a specific interval after BRXFS signal is asserted and when the BRXFS signal is de-asserted.

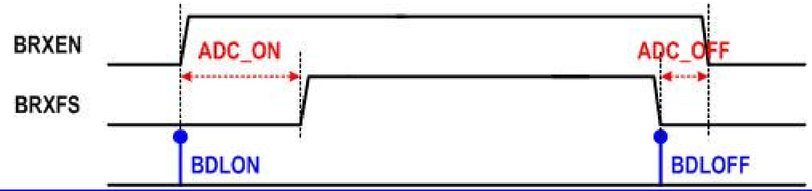

Figure 52 The timing diagram of BRXEN and BRXFS

Note: TDMA_BDLON/OFF event registers, together with TDMA_BDLCON register, generate the corresponding BRXEN and BRXFS window used to power up/down baseband downlink path and control the duration of data transmission to the DSP, respectively.

On-chip Transmit Events

TDMA_APC [1:0]

These registers initiate the loading of the transmit burst shaping values from the transmit burst shaping RAM into the transmit power control DAC.

TDMA_BULON [0]

This register contains the quarter bit event that initiates the transmit window assertion sequence which powers up the modulator DAC and then enables reading of bits from the transmit buffer into the GMSK modulator.

TDMA_BULOFF [0]

This register contains the quarter bit event that initiates the transmit window de-assertion sequence which disables the reading of bits from the transmit buffer into the GMSK modulator, and then power down the modulator DAC.

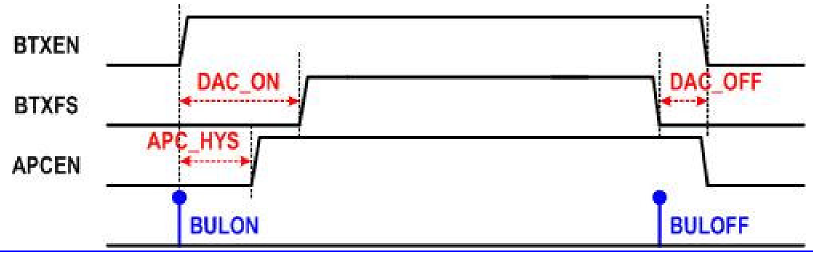

Figure 53 The timing diagram of BTXEN and BTXFS

Note: TDMA_BULON/OFF event registers, together with TDMA_BULCON1, TDMA_BULCON2 register, generate the corresponding BTXEN, BTXFS and APCEN window used to power up/down the baseband uplink path, control the duration of data transmission from the DSP and power up/down the APC DAC, respectively.

Off-chip Control Events

TDMA_BSI [12:0]

The quarter bit positions of these 13 BSI events are used to initiate the transfer of serial words to the transceiver and synthesizer for gain control, frequency adjustment.

TDMA_BPI [12:0]

The quarter bit positions of these 13 BPI events are used to generate changes of state on the output pins to control the external radio components.

8.1.1 Register Definitions

TDMA+0150h Event enable register 0 — TDMA_EVTENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFC3	AFC2	AFC1	AFC0			BDL3	BDL2	BDL1	BDL0				CTIRQ2	CTIRQ1	DTIRQ
Type	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W				R/W	R/W	R/W
Reset	0	0	0	0			0	0	0	0				0	0	0

DTIRQ Enable TDMA_DTIRQ

CTIRQ*n* Enable TDMA_CTIRQ*n*

AFC*n* Enable TDMA_AFC*n*

BDL*n* Enable TDMA_BDLON*n* and TDMA_BDLOFF*n*

For all these bits,

0 function is disabled

1 function is enabled

TDMA+0154h Event enable register 1 — TDMA_EVTENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUL0					APC1	APC0
Type										R/W					R/W	R/W
Reset										0					0	0

APC*n* Enable TDMA_APC*n*

BUL*n* Enable TDMA_BULON*n* and TDMA_BULOFF*n*

For all these bits,

0 function is disabled

1 function is enabled

TDMA +0158h Event enable register 2 TDMA_EVTENA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

BSI*n* BSI event enable control

0 Disable TDMA_BSI*n*

1 Enable TDMA_BSI*n*

TDMA +015Ch Event enable register 3 TDMA_EVTENA3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BPI12	BPI11	BPI10	BPI9	BPI8	BPI7	BPI6	BPI5	BPI4	BPI3	BPI2	BPI1	BPI0
Type				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

BPI*n* BPI event enable control

0 Disable TDMA_BPI*n*

1 Enable TDMA_BPI*n*

TDMA +0170h Qbit Timer Offset Control Register TDMA_WRAPOFS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TOI[1:0]	
Type															R/W	
Reset															0	

TOI This register defines the value used to advance the Qbit timer in unit of 1/4 quarter bit; the timing advance will be taken place as soon as the TDMA_EVTVAL is occurred, and it will be cleared automatically.

TDMA +0174h Qbit Timer Biasing Control Register TDMA_REGBIAS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TQ_BIAS[13:0]													
Type			R/W													
Reset			0													

TQ_BIAS This register defines the Qbit offset value which will be added to the registers being programmed. It only takes effects on AFC, BDLON/OFF, BULON/OFF, APC, BSI and BPI event registers.

TDMA +0180h DTX control register — TDMA_DTXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DTX0
Type																R/W

DTX DTX flag is used to disable the associated transmit signals

- **0** BULON0, BULOFF0, APC_EV0 & APC_EV1 are controlled by TDMA_EVTENA1 register
- **1** BULON0, BULOFF0, APC_EV0 & APC_EV1 are disabled

TDMA +0184h Receive interrupt control register — TDMA_RXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MOD3	MOD2	MOD1	MOD0	RXINTCNT[9:0]									
Type			R/W	R/W	R/W	R/W	R/W									

RXINTCNT TDMA_RXWIN interrupt generation interval in quarter bit unit

MODn [Description for this register field]

- **0** Single shot mode for the corresponding receive window
- **1** Repetitive mode for the corresponding receive window

TDMA +0188h Baseband downlink control register — TDMA_BDLCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_ON										ADC_OFF					
Type	R/W										R/W					

ADC_ON BRXEN to BRXFS setup up time in quarter bit unit.

ADC_OFF BRXEN to BRXFS hold up time in quarter bit unit.

TDMA +018Ch Baseband uplink control register 1 — TDMA_BULCON 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAC_ON										DAC_OFF					
Type	R/W										R/W					

DAC_ON BTXEN to BTXFS setup up time in quarter bit unit.

DAC_OFF BTXEN to BTXFS hold up time in quarter bit unit.

TDMA +0190h Baseband uplink control register 2 — TDMA_BULCON 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									APC_HYS							
Type									R/W							

APC_HYS APCEN to BTXEN hysteresis time in quarter bit unit.

Address	Type	Width	Reset Value	Name	Description
+0000h	R	[13:0]	—	TDMA_TQCNT	Read quarter bit counter
+0004h	R/W	[13:0]	0x1387	TDMA_WRAP	Latched Qbit counter reset position
+0008h	R/W	[13:0]	0x1387	TDMA_WRAPIMD	Direct Qbit counter reset position
+000Ch	R/W	[13:0]	0x0000	TDMA_EVTVAL	Event latch position
+0010h	R/W	[13:0]	—	TDMA_DTIRQ	DSP software control

+0014h	R/W	[13:0]	—	TDMA_CTIRQ1	MCU software control 1
+0018h	R/W	[13:0]	—	TDMA_CTIRQ2	MCU software control 2
+0020h	R/W	[13:0]	—	TDMA_AFC0	The 1st AFC control
+0024h	R/W	[13:0]	—	TDMA_AFC1	The 2nd AFC control
+0028h	R/W	[13:0]	—	TDMA_AFC2	The 3rd AFC control
+002Ch	R/W	[13:0]	—	TDMA_AFC3	The 4th AFC control
+0030h	R/W	[13:0]	—	TDMA_BDLON0	Data serialization of the 1st RX block
+0034h	R/W	[13:0]	—	TDMA_BDLOFF0	
+0038h	R/W	[13:0]	—	TDMA_BDLON1	Data serialization of the 2nd RX block
+003Ch	R/W	[13:0]	—	TDMA_BDLOFF1	
+0040h	R/W	[13:0]	—	TDMA_BDLON2	Data serialization of the 3rd RX block
+0044h	R/W	[13:0]	—	TDMA_BDLOFF2	
+0048h	R/W	[13:0]	—	TDMA_BDLON3	Data serialization of the 4th RX block
+004Ch	R/W	[13:0]	—	TDMA_BDLOFF3	
+0060h	R/W	[13:0]	—	TDMA_BULON0	Data serialization of the 1st TX slot
+0064h	R/W	[13:0]	—	TDMA_BULOFF0	
+0090h	R/W	[13:0]	—	TDMA_APC0	The 1st APC control
+0094h	R/W	[13:0]	—	TDMA_APC1	The 2nd APC control
+00B0h	R/W	[13:0]	—	TDMA_BSI0	BSI event 0
+00B4h	R/W	[13:0]	—	TDMA_BSI1	BSI event 1
+00B8h	R/W	[13:0]	—	TDMA_BSI2	BSI event 2
+00BCh	R/W	[13:0]	—	TDMA_BSI3	BSI event 3
+00C0h	R/W	[13:0]	—	TDMA_BSI4	BSI event 4
+00C4h	R/W	[13:0]	—	TDMA_BSI5	BSI event 5
+00C8h	R/W	[13:0]	—	TDMA_BSI6	BSI event 6
+00CCh	R/W	[13:0]	—	TDMA_BSI7	BSI event 7
+00D0h	R/W	[13:0]	—	TDMA_BSI8	BSI event 8
+00D4h	R/W	[13:0]	—	TDMA_BSI9	BSI event 9
+00D8h	R/W	[13:0]	—	TDMA_BSI10	BSI event 10
+00DCh	R/W	[13:0]	—	TDMA_BSI11	BSI event 11
+00E0h	R/W	[13:0]	—	TDMA_BSI12	BSI event 12
+0100h	R/W	[13:0]	—	TDMA_BPI0	BPI event 0
+0104h	R/W	[13:0]	—	TDMA_BPI1	BPI event 1
+0108h	R/W	[13:0]	—	TDMA_BPI2	BPI event 2
+010Ch	R/W	[13:0]	—	TDMA_BPI3	BPI event 3
+0110h	R/W	[13:0]	—	TDMA_BPI4	BPI event 4
+0114h	R/W	[13:0]	—	TDMA_BPI5	BPI event 5
+0118h	R/W	[13:0]	—	TDMA_BPI6	BPI event 6
+011Ch	R/W	[13:0]	—	TDMA_BPI7	BPI event 7
+0120h	R/W	[13:0]	—	TDMA_BPI8	BPI event 8
+0124h	R/W	[13:0]	—	TDMA_BPI9	BPI event 9
+0128h	R/W	[13:0]	—	TDMA_BPI10	BPI event 10
+012Ch	R/W	[13:0]	—	TDMA_BPI11	BPI event 11
+0130h	R/W	[13:0]	—	TDMA_BPI12	BPI event 12
+0150h	R/W	[10:0]	0x0000	TDMA_EVTENA0	Event Enable Control 0
+0154h	R/W	[6,1:0]	0x0000	TDMA_EVTENA1	Event Enable Control 1
+0158h	R/W	[12:0]	0x0000	TDMA_EVTENA2	Event Enable Control 2
+015Ch	R/W	[12:0]	0x0000	TDMA_EVTENA3	Event Enable Control 3
+0170h	R/W	[1:0]	0x0000	TDMA_WRAPOFS	TQ Counter Offset Control Register
+0174h	R/W	[13:0]	0x0000	TDMA_REGBIAS	Biasing Control Register

+0180h	R/W	[0]	—	TDMA_DTXCON	DTX Control Register
+0184h	R/W	[13:0]	—	TDMA_RXCON	Receive Interrupt Control Register
+0188h	R/W	[15:8, 5:0]	—	TDMA_BDLCON	Downlink Control Register
+018Ch	R/W	[15:8, 5:0]	—	TDMA_BULCON1	Uplink Control Register 1
+0190h	R/W	[15:8]	—	TDMA_BULCON2	Uplink Control Register 2

Table 35 TDMA Timer Register Map

8.2 Slow Clocking Unit

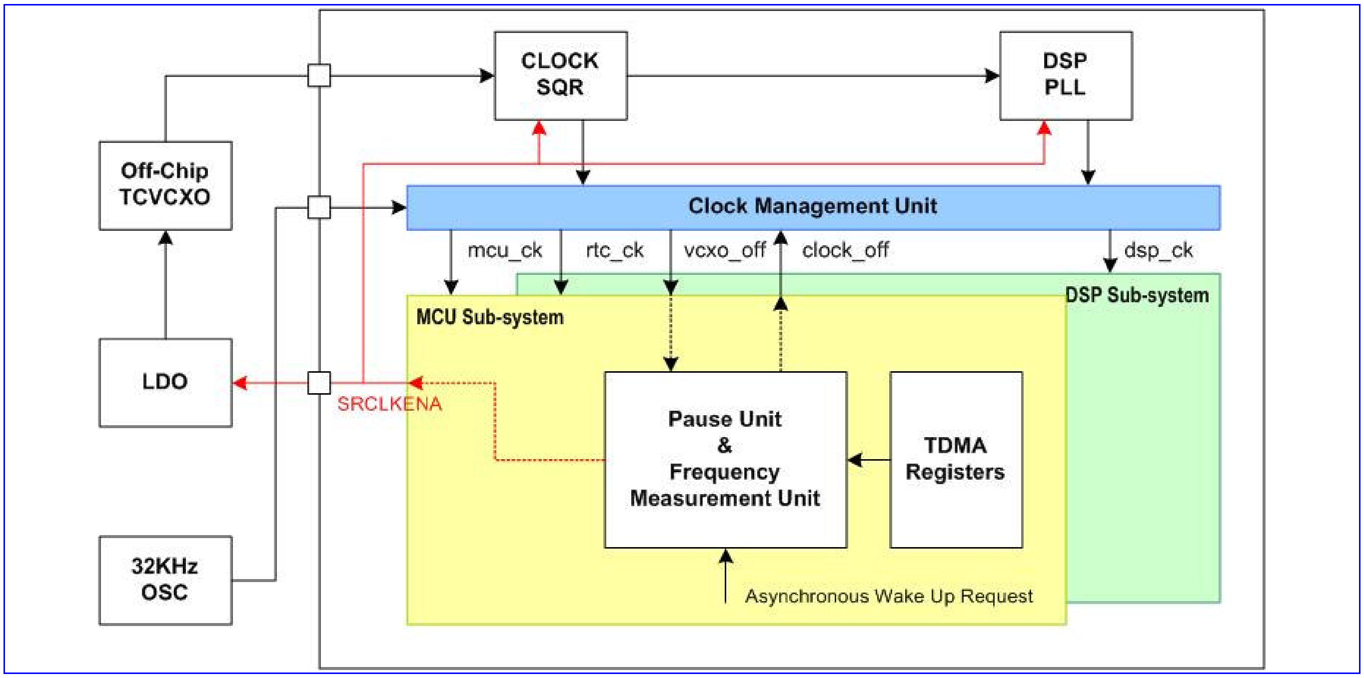

Figure 54 The block diagram of the slow clocking unit

The slow clocking unit is provided to maintain the synchronization to the base-station timing using a 32KHz crystal oscillator while the 13MHz reference clock is switched off. As shown in Figure 54, this unit is composed of frequency measurement unit, pause unit and clock management unit.

Because of the inaccuracy of the 32KHz oscillator, a frequency measurement unit is provided to calibrate the 32KHz crystal taking the accurate 13MHz source as the reference. The calibration procedure always takes place prior to the pause period.

The pause unit is used to initiate and terminate the pause mode procedure and it also works as a coarse time-base during the pause period.

The clock management unit is used to control the system clock while switching between the normal mode and the pause mode. SRCLKENA is used to turn on/off the clock squarer, DSP PLL and off-chip TCVCXO. CLOCK_OFF signal is used for gating the main MCU and DSP clock , and VCXO_OFF is used as the acknowledge signal of the CLOCK_OFF request.

8.2.1 Register Definitions

TDMA +0218h Slow clocking unit control register **SM_CON**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE_START	FM_START
Type															W	W
Reset															0	0

FM_START Initiate the frequency measurement procedure

PAUSE_START Initiate the pause mode procedure at the next timer wrap position

TDMA +0220h Slow clocking unit status register **SM_STA**

Bit	15	14	13	12	11	10	9	8
Name								PAUSE_ABORT
Type								R
Bit	7	6	5	4	3	2	1	0
Name	SETTLE_CPL	PAUSE_CPL	PAUSE_INT	PAUSE_RQST			FM_CPL	FM_RQST
Type	R	R	R	R			R	R

FM_RQST Frequency measurement procedure is requested

FM_CPL Frequency measurement procedure is completed

PAUSE_RQST Pause mode procedure is requested

PAUSE_INT Asynchronous wake up from pause mode

PAUSE_CPL Pause period is completed

SETTLE_CPL Settling period is completed

PAUSE_ABORT Pause mode is aborted because of the reception of interrupt prior to entering pause mode

TDMA +022Ch Slow clocking unit configuration register **SM_CNF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EINT	KP	SM	FM
Type													R/W	R/W	R/W	R/W
Reset													0	0	1	1

FM Enable interrupt generation upon completion of frequency measurement procedure

SM Enable interrupt generation upon completion of pause mode procedure

KP Enable asynchronous wake-up from pause mode by key press

EINT Enable asynchronous wake-up from pause mode by external interrupt

Address	Type	Width	Reset Value	Name	Description
+0200h	R/W	[0]	—	SM_PAUSE_M	MSB of pause duration
+0204h	R/W	[15:0]	—	SM_PAUSE_L	16 LSB of pause duration
+0208h	R/W	[13:0]	—	SM_CLK_SETTLE	Off-chip VCXO settling duration
+020Ch	R	[0]	—	SM_FINAL_PAUSE_M	MSB of final pause count
+0210h	R	[15:0]	—	SM_FINAL_PAUSE_L	16 LSB of final pause count
+0214h	R	[13:0]	—	SM_QBIT_START	TQ_ COUNT value at the start of the pause
+0218h	W	[1:0]	0x0000	SM_CON	SM control register
+021Ch	R	[7:3,1:0]	0x0000	SM_STA	SM status register

+0220h	R/W	[15:0]	—	SM_FM_DURATION	32KHz measurement duration
+0224h	R	[9:0]	—	SM_FM_RESULT_M	10 MSB of frequency measurement result
+0228h	R	[15:0]	—	SM_FM_RESULT_L	16 LSB of frequency measurement result
+022Ch	R/W	[3:0]	0x0000	SM_CNF	SM configuration register

8.2.2 Frequency Measurement

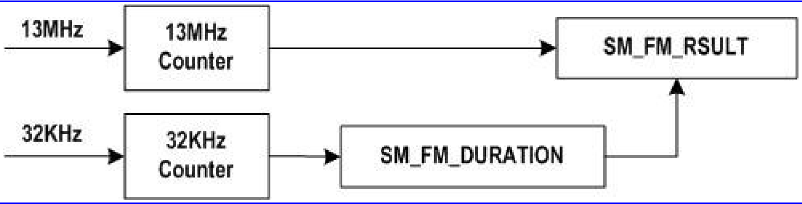

Figure 55 Block Diagram of Frequency Measurement Unit

The MCU writes into the SM_FM_DURATION register the number of clock cycles, during which the 32768 Hz clock will be measured. Then, the MCU sets the FM_START bit in the SM_CON register, the hardware sets the FM_RQST flag and resets the FM_CPL flag automatically and the 32kHz and 13MHz counters are simultaneously started from zero.

When the 32kHz counter reaches the terminal value determined by the SM_FM_DURATION register, the current value of the 13MHz counter is stored in the SM_FM_RESULT register, the counters are stopped , the FM_RQST is reset and the FM_CPL flag is set.

The SM_FM_DURATION is 16 bits wide, and the 32K counter counts $2 \times (N+1)$ cycles of 32768Hz. This gives a maximum of almost 4.00s measurement duration.

$$Measured_frequency = \frac{2 \times (SM_FM_DURATION + 1) \times 13 \times 10^6}{SM_FM_RESULT}$$

8.2.3 Pause Mode Operation

The MCU writes the pause and settling time into the SM_PAUSE_M, SM_PAUSE_L and SM_CLK_SETTLE registers and the sum of the pause time and settling time must be as close as possible to the TDMA frame boundary, taking into account the frequency measurement result.

The MCU should set the PAUSE_START bit ahead of the TDMA_EVTVAL event. The hardware sets the PAUSE_RQST flag and resets the PAUSE_INT, PAUSE_CPL, SETTLE_CPL, PAUSE_ABORT flags automatically and the pause mode operation will be initiated at the next timer wrap position.

When the pause duration reaches the programmed terminal value or the asynchronous wake up event is received, the pause mode operation is ended/stopped/aborted and the corresponding flag is set (PAUSE_CPL, PAUSE_INT and PAUSE_ABORT). Then, the MCU calculates the timing offset and adjusts the TDMA_WRAPIMD position accordingly.

The number of quarter bit time elapsed during the pause operation is:

$$Nb_quarter_bit = Kqbit \times (SM_FINAL_PAUSE + SM_CLK_SETTLE) - \Delta qbit$$

$$\Delta qbit = TQ_WRAP - SM_QBIT_START$$

$$Kqbit = \frac{32k_period_duration}{quarter_bit_duration} = \frac{SM_FM_RESULT}{24 \times (SM_FM_DURATION + 1)}$$

9 Power, Clocks and Reset

This chapter describes about the power, clock and reset management functions provided by MT6205B. Together with Power Management IC (PMIC), MT6205B offers both fine and coarse resolutions of power control by software programming. With this efficient method, the developer can turn on selective resources accordingly in order to achieve optimized power consumption. The operating modes of MT6205B as well as main power states provided by PMIC are shown in **Figure** 56.

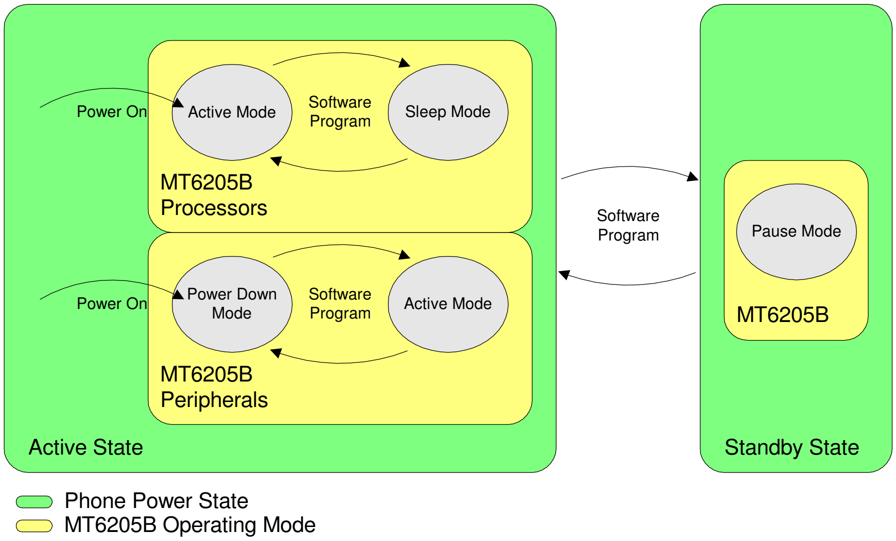

Figure 56 Major Phone Power States and Operating Modes for MT6205B based terminal

9.1 Power Management

9.1.1 General Description

To provide steady supply sources and to save the unnecessary power consumption, a dedicated power management IC (PMIC) designed for MT6205B to meet those requirements. In general, the PMIC must fulfill the following features:

- Low drop-out regulators.
- Power-on reset and start-up timer.
- Battery charging circuits
- Under/over voltage lock-up protection circuits as well as thermal overload protections.

Total 7 LDOs are required: digital core circuit(**VDDK**), digital IO(**VDD33**), analog and mixed signal(**AVDD_xxx**), RTC(**AVDDRTC**), EMI(**VDD33_EMI**), SIM(**SIMVCC**), and the 13MHz clock source (**AVDD_PLL**). **Table 36** lists the relative ON/OFF states of different handset states. Table 37 explains the power management states of the handset.(*[2])

[2] For detailed power management information, refer to the document “Functional Requirement of Power Management”.

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Phone Power State	Charger ON	Under Voltage Lock-up	Power key press	**SRCLKENA** (13MHz enable)	**AVDDRTC**	**AVDD_PLL, AVDD_xxx**	Digital Supplies
$\mathbf{V_{BAT}}$<2.5V	X	L	X	X	Off	Off	Off
2.5V<$\mathbf{V_{BAT}}$<3.2V	L	L	X	X	On	Off	Off
Pre-charging	H	L	X	X	On	Off	Off
Charger-on	H	H	X	X	On	On	On
Switched Off	L	H	L	X	On	Off	Off
Standby	L	H	H	L	On	Off	On
Active	L	H	H	H	On	On	On

Table 36 State table of different phone states and LDO switches.

States	Description
Phone Power Off	No battery connected or battery connected but the battery is deep discharged, i.e. $\mathbf{V_{BAT}}$ < 3.2V, at this state, no LDO should be enabled except **AVDDRTC**. **AVDDRTC** should only be disabled when $\mathbf{V_{BAT}}$<2.5V.
Phone Switched Off	Phone is connected with battery but is switched off. The battery voltage is higher than 3.2V. At this state, **AVDDRTC** is enabled while all other LDOs are disabled.
Pre-Charging	The charger is connected to the mobile, but $\mathbf{V_{BAT}}$<3.2V. Slow charging is activated with charger circuits in PMIC. Upon $\mathbf{V_{BAT}}$ is charged up to 3.2V, and then detection circuit in PMIC will enable normal charging, pull –UV (under voltage) signal high and enable all LDO outputs.
Standby	The handset is powered up but the 13MHz reference clock was disabled, 32kHz clock parts of the baseband chip is running.
Active	Phone is powered up and is running with 13MHz reference clock. All LDOs are enabled, and mobile radio tasks are running.
Active Alarm	The mobile is waken-up via RTC alarm, all LDOs are enabled but only the alarm task is scheduled; no radio activities are scheduled.
Switched Off / Charging	The mobile has charger connected, baseband is active and running on 13MHz reference clock but only charging software is scheduled, neither radio nor MMI tasks are activated. LCD screen should show battery charging status only.
Active / Charging	The mobile has charger connected, baseband process is active and running on 13MHz reference clock with regular mobile radio and MMI task activated. LCD screen shows battery charging status plus all normal tasks.

Table 37 Explanation of the phone states.

Three events can wake-up the handset: User presses the power key, charger connection, and RTC BBWAKEUP. Power key press is detected both by the PMIC and MT6205B. Charger connection is firstly detected by the PMIC and it then informs MT6205B that the charger connects; after the baseband chip wakes up, it takes the duty of charging control by monitoring the charging status through the auxiliary ADC. The control signal is sent to the PMIC as CHR_CNTL, usually a GPIO pin. RTC BBWAKEUP is issued by the RTC region of MT6205B as a time-up event. Besides, a 13MHz clock enable signal SRCLKENA is sent from the sleep unit inside MT6205B to power up/down the CTXO LDO. The baseband chip also has to monitor the status of the battery: the battery voltage, temperature, and type. Also, for emergency events such as battery

suddenly removed, an interrupt will be issued from the PMIC to the external interrupt interface of baseband chip. **Figure 57** shows the connections between the PMIC and the baseband chip.

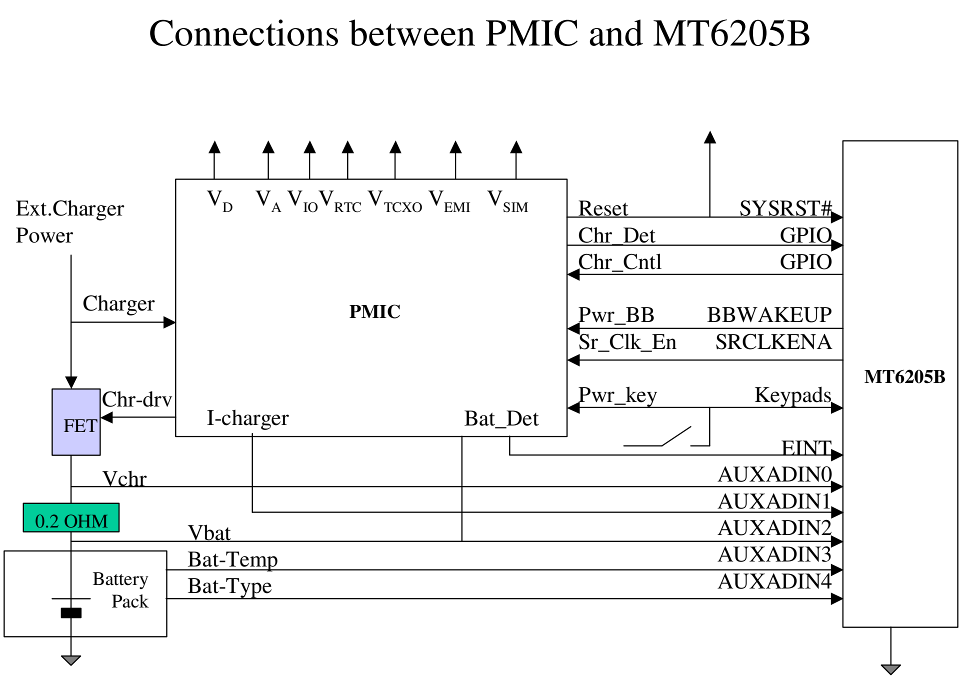

Figure 57 Typical PMIC and MT6205B baseband chip connections. The auxiliary ADC input order depends on application and can be swapped. In system view, the PMIC also takes responsibility of buzzer, vibrator and LED driving power supply.

9.2 Clocks

There are two major time bases in the MT6205B. For the faster one is the 13 MHz Time Base originating from an off-chip temperature-compensated voltage controlled oscillator (TCVCXO) that can be either 13MHz or 26MHz. This signal is input from the SYSCLK pad then is converted to the square-wave signal. The other time base is the 32768 Hz clock generated by an on-chip oscillator connected to an external crystal. **Figure 58** shows the clock sources as well as their utilizations inside the chip.

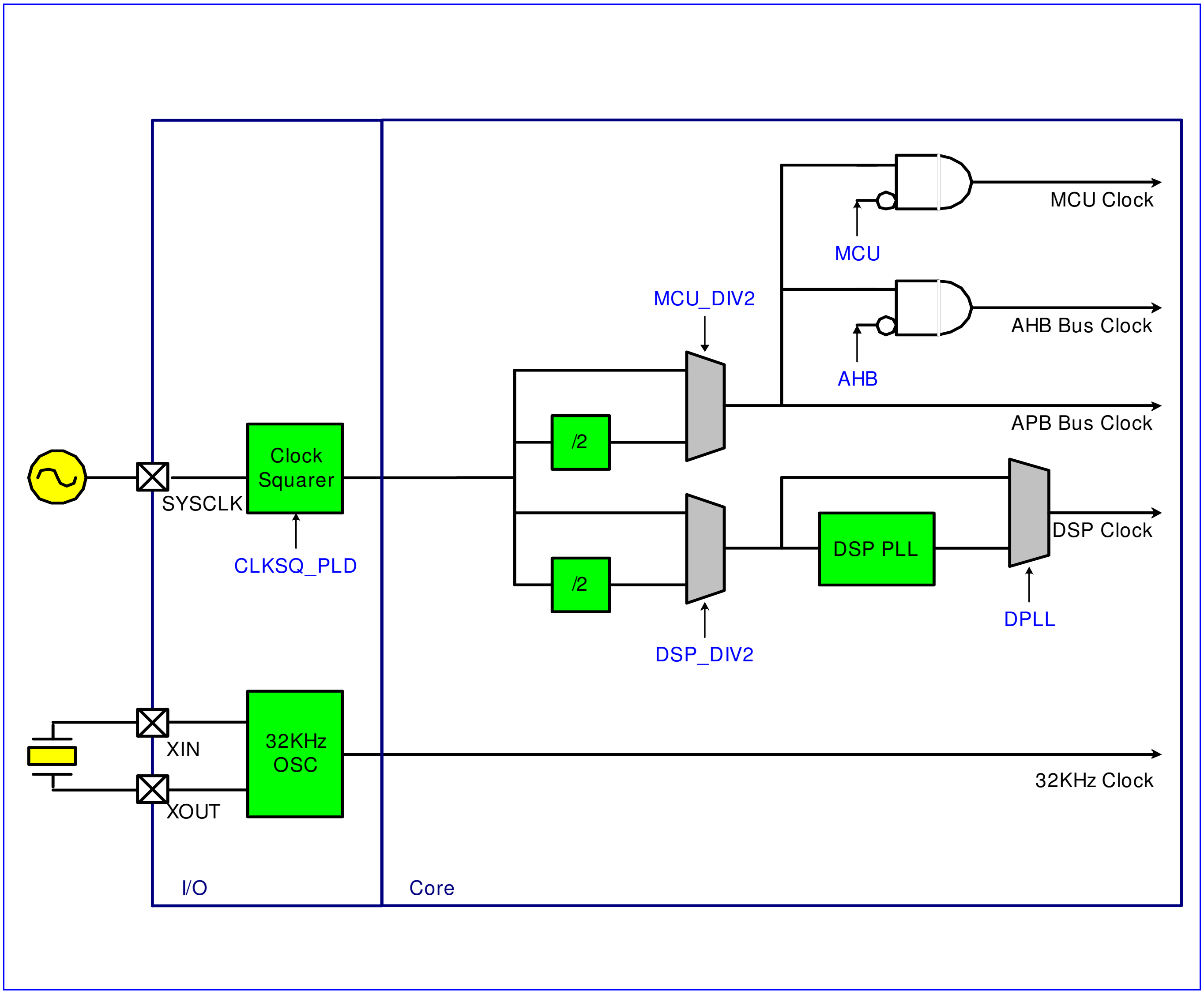

Figure 58 Clock distributions inside the MT6205B

9.2.1 32.768 KHz Time Base

The 32768 Hz clock will be always running. Its primary usage is used as the time base of the Real Time Clock (RTC) module, which maintains time and date with counters. Therefore, both the 32768Hz oscillator and the RTC module will be powered by a separate voltage supply that wouldn't power down when the other supplies do.

In low power mode, the 13 MHz time base is turned off, so the 32768 Hz clock shall be employed to update the critical TDMA timer and Watchdog Timer. The keypad scanner logic is also clocked by this time base.

9.2.2 13 MHz Time Base

Two 1/2-dividers, one for MCU Clock and one for DSP Clock, are exist to allow using 26 or 13 MHz TCVCXO. One phase-locked loops, DPLL, is used to generate the DSP primary clock, DSP Clock, for modules in DSP Clock Domain. The DPLL requires no off-chip components for operations and can be turn off independently in order to save power. After

power-on, the DPLL is off by default and the source clock signal is selected through the multiplexer. The software shall take cares of the PLL lock time while changing the clock selections.

The DPLL can be programmed to provide 1X to 4X output of the 13 MHz reference. The MCU software program may set the clock multiplier according to the DSP performance required. Currently, for this version of chip the multiply factor will be set to 4X.

For power management, the MCU software program may stop MCU Clock or AHB Bus Clock by setting the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode, thus return to the running mode.

9.2.3 Register Definitions

CONFIG+100h MCU Frequency register — MCU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FSEL
Type																R/W
Reset																0

FSEL While the external clock source is 26MHz, this bit could be set to 1 of allowing the MCU running at 26MHz.

- **0** MCU is running at 13MHz
- **1** MCU is running at 26MHz

CONFIG+104h DPLL Frequency register — DPLL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CALI					RST						SPD	
Type				R/W					R/W						R/W	
Reset				0					0						0	

SPD Select the Output Speed Rate for DPLL

- **00** power down
- **01** 13MHz x 2
- **10** 13MHz x 3
- **11** 13MHz x 4

RST Reset Control of DPLL

- **0** Normal Oprtation
- **1** Reset the DPLL

CALI Calibration Control for DPLL

CONFIG+108h Clock Control Register — CLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DPLL_TMA	CLKSQ_PLD	MCU_DIV2	DPLL		DSP_DIV2
Type											R/W	R/W	R/W	R/W		R/W
Reset											0	0	0	0		0

DSP_DIV2 Control the x2 clock divider for DPLL input

- **0** Divider bypassed
- **1** Divider not bypassed

DPLL Select DSP Clock

0 DPLL bypassed
1 Using DPLL Clock

MCU_DIV2 Control the x2 clock divider for MCU clock domain
0 Divider bypassed
1 Divider not bypassed

CLKSQ_PLD Pull Down Control
0 Disable
1 Enables

DPLL_TMA DPLL test mode
0 Disable
1 Enables

CONFIG+10Ch Sleep Control Register SLEEP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AHB	MCU
Type															W	W
Reset															0	0

MCU Stop the MCU Clock to force MCU Processor entering sleep mode. MCU clock will be resumed as long as there comes an interrupt request or system is reset.
0 MCU Clock is running
1 MCU Clock is stopped

AHB Stop the AHB Bus Clock to force the entire bus entering sleep mode. AHB Bus clock will be resumed as long as there comes an interrupt request or system is reset.
0 AHB Bus Clock is running
1 AHB Bus Clock is stopped

9.3 Reset Management

Figure 59 shows reset scheme used in MT6205B. There are three kinds of resets in the MT6205B, i.e., hardware reset, watchdog reset, and software resets.

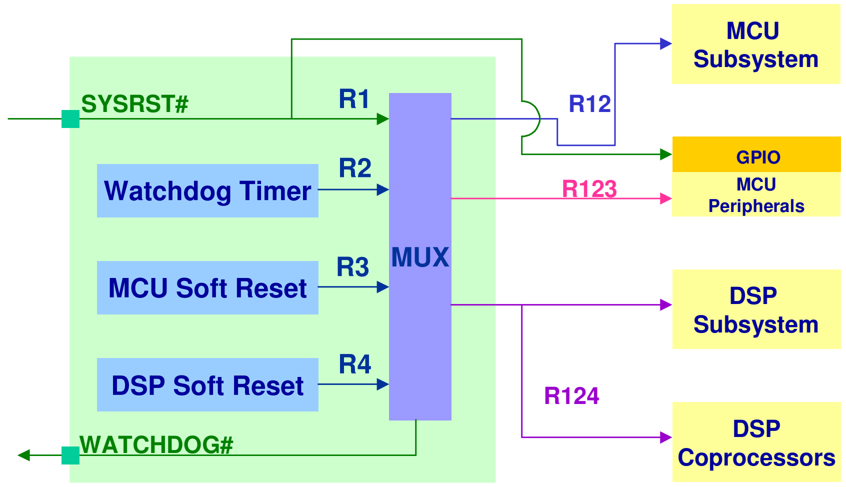

Figure 59 Reset Scheme Used in MT6205B

9.3.1 General Description

9.3.1.1 Hardware Reset

This reset is input through the SYSRST# pin, which shall be driven to low during power-on. The hardware reset has a global effect on the chip: it initializes all digital and analog circuits except the Real Time Clock module. The initial states of the MT6205B sub-blocks are listed below.

- All analog circuits are turned off.
- All PLLs are turned off and bypassed. The 13MHz system clock is the default time base.
- Special Trap States in GPIO

9.3.1.2 Watchdog Reset

A watchdog reset is generated when the Watchdog Timer expires as the MCU software failed to re-program the timer counter in time. This situation is typically induced by abnormal software execution, which can be aborted by a hardwired watchdog reset. Hardware blocks that are affected by the watchdog reset are

- MCU subsystem
- DSP subsystem
- External Components (by software program)

9.3.1.3 Software Resets

These are local reset signals that initialize specific hardware. The MCU or DSP software may write to software reset trigger registers to return hardware modules to their initial states, when hardware failures are detected, for example.

The following modules have software resets.

- MCU Peripherals
- DSP Core

- DSP Coprocessors

9.3.2 Register Definitions

RGU +0000h Watchdog Timer Control register WDT_MODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[7:0]													EXTEN	EXTPOL	ENABLE
Type														R/W	R/W	R/W
Reset														0	0	0

ENABLE

0 Disable Watchdog Timer

1 Enable Watchdog Timer

EXTPOL Define the polarity of the external watchdog pin

0 Active low

1 Active high

EXTEN

0 The watchdog can not generate an external watchdog reset signal

1 If the watchdog counter reaches zero, an external watchdog signal is generated

KEY Write access is allowed if KEY=0x22

RGU +0004h Watchdog Time-Out Interval register WDT_LENGTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMOUT[7:0]								KEY[7:0]							
Type	W															
Reset	1111_1111b															

KEY Write access is allowed if KEY=08h

TIMOUT The counter is restarted with {TIMEOUT [7:0], 1_1111_1111b}. So the Watchdog Timer time-out period is a multiple of 512*T_{32k}=15.6ms

RGU +0008h Watchdog Timer Restart register WDT_RESTART

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type																
Reset																

KEY Restart the counter if KEY=1971h

RGU +000Ch Watchdog Timer Status register WDT_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STA															
Type	R															
Reset	0															

STA

0 Reset not due to Watchdog Timer

1 Reset due to that Watchdog Timer time-out period is reached

NOTE: The system reset does not affect this register. This bit is cleared when the bit ENABLE of WTU_MODE register is written.

RGU +0010h CPU Peripheral Software Reset Register SW_PERIPH_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET	DAMRST														
Type	R/W	R/W														
Reset	0	0														

RESET Controls the APB Peripherals Reset Control

0: No Reset

1: Reset Activated

DMARST Reset the DMA peripheral

0: No Reset

1: Reset Activated

RGU +0014h DSP Software Reset Register SW_DSP_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST															
Type	R/W															
Reset	0															

RST Controls the DSP System Reset Control

0: No reset

1: Reset activate

RGU +0018h Watchdog Timer Reset Signal Duration register WDT_RSTINTREVAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LENGTH[11:0]											
Type					R/W											
Reset					FFFh											

LENGTH This register indicates the reset duration when watchdog timer timeout

9.4 Software Power Down Control

In addition to have Pause Mode at Standby State, the software program can also put each peripherals independently in Power Down Mode at Active State by gating their clock off. The typical logic implemented is described as **Figure 60**. For all these configuration bits, 1 means that the function is Power Down Mode and 0 means that it is in the Active Mode.

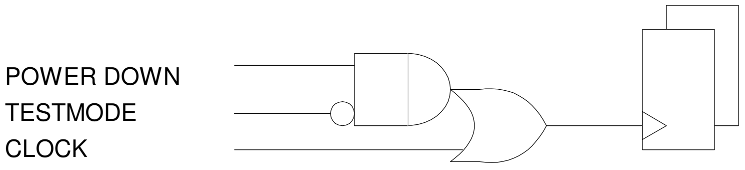

Figure 60 Power Down Control at Block Level

9.4.1 Register Definitions

CONFIG+300h Power Down Control 0 Register — PDN_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		DPLL	MCU_DIV2	CLKSQ											DMA
Type	R/W		R/W	R/W	R/W											R/W
Reset	1		1	1	0											1

DMA Controls the DMA Controller Power Down
CLKSQ Controls the Clock squarer Power Down
MCU_DIV2 Controls the MUC DIV2 Power Down
DPLL Controls the DPLL Power Down
DSP_DIV2 Controls the DSP DIV2 Power Down

CONFIG +304h Power Down Control 1 Register — PDN_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PWM2	MMC	UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						1	1	1	1	1	1	1	1	1	1	1

GPT Controls the General Purpose Timer Power Down
KP Controls the Keypad Scanner Power Down
GPIO Controls the GPIO Power Down
UART1 Controls the UART1 Controller Power Down
SIM Controls the SIM Controller Power Down
PWM1 Controls the PWM Generator Power Down
ALTER Controls the Alerter Generator 1 Power Down
LCD Controls the Serial LCD Controller Power Down
UART2 Controls the UART2 Controller Power Down
MMC Controls the MMC Controller Power Down
PWM2 Controls the PWM Generator 2 Power Down

CONFIG +308h Power Down Control 2 Register — PDN_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX			DIV	GCC	BFE	AFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	R/W	R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1			1	1	1	1	1	1	1	1	1	1	1	1

TDMA Controls the TDMA Power Down
BSI Controls the BSI Power Down
BPI Controls the BPI Power Down
AFC Controls the AFC Power Down
APC Controls the APC Power Down
FCS Controls the FCS Power Down
AUXAD Controls the AUX ADC Power Down
AFE Controls the Audio Front End Power Down
BFE Controls the Base-Band Front End Power Down
GCC Controls the GCC Power Down
DIV Controls the Divider Power Down
BBRX Controls the BB RX Power Down
GMSK Controls the GMSK Power Down

CONFIG +30Ch Power Down Control 3 Register PDN_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDMA ALIGN															ICE
Type	R/W															R/W
Reset	0															1

ICE Enables the debug feature of the ARM7TDMI core. It controls the DBGEN pin of the ICEBreaker.
TDMA_ALIGN Enables the alignment control of power up and down sequences for APC, AFC, BPI and BSI
0 No alignment control with TDMA Timer
1 Aligned with TDMA Q-Bit Counter

CONFIG +310h Set Control for Power Down Control 0 Register PDN_CON0_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		DPLL	MCU_DIV2	CLKSQ											DMA
Type	WS		WS	WS	WS											WS

CONFIG +314h Set Control for Power Down Control 1 Register PDN_CON1_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								UART2	LCD	ALTER	PWM	SIM	UART1	GPIO	KP	GPT
Type								WS	WS	WS	WS	WS	WS	WS	WS	WS

CONFIG +318h Set Control for Power Down Control 2 Register PDN_CON2_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX			DIV	GCC	BFE	AFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA

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Type	WS	WS			WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS	WS

CONFIG +31Ch Set Control for Power Down Control 3 Register PDN_CON3_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDMA ALIGN															ICE
Type	WS															WS

This register is used to set bits in the corresponding Power Down Control Registers. When writing to this register each data bit which is “1” will cause the corresponding bit in the Power Down Control Register to be set to “1”. Data bits which are “0” have no effect on the corresponding bit in the Power Down Control Register.

CONFIG +320h Clear Control for Power Down Control 0 Register PDN_CON0_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		DPLL	MCU_DIV2	CLKSQ											DMA
Type	WC		WC	WC	WC											WC

CONFIG +324h Clear Control for Power Down Control 1 Register PDN_CON1_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM2	UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type							WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

CONFIG +328h Clear Control for Power Down Control 2 Register PDN_CON2_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX			DIV	GCC	BFE	AFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	WC	WC			WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

CONFIG +32Ch Clear Control for Power Down Control 3 Register PDN_CON3_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDMA ALIGN															ICE
Type	WC															WC

This register is used to clear bits in the corresponding Power Down Control Registers. When writing to this register each data bit which is “1” will causes the corresponding bit in the Power Down Control Register to be cleared to “0”. Data bits which are “0” have no effect on the corresponding bit in the Power Down Control Register.

CONFIG +330h Power Down Control 4 Register PDN_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name											APC	AFC	BPI	BSI		
Type											R/W	R/W	R/W	R/W		
Reset											1	1	1	1		

BSI Controls the BSI Power Down based on TDMA Timer. Controlled by the TDMA_ALIGN bit of PDN_CON3.

BPI Controls the BPI Power Down based on TDMA Timer. Controlled by the TDMA_ALIGN bit of PDN_CON3.

AFC Controls the AFC Power Down based on TDMA Timer. Controlled by the TDMA_ALIGN bit of PDN_CON3.

APC Controls the APC Power Down based on TDMA Timer. Controlled by the TDMA_ALIGN bit of PDN_CON3.

CONFIG +334h Set Control for Power Down Control 4 Register PDN_CON4_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											APC	AFC	BPI	BSI		
Type											WS	WS	WS	WS		

This register is used to set bits in the Power Down Control Register 4. When writing to this register each data bit which is "1" will cause the corresponding bit in the Power Down Control Register to be set to "1". Data bits which are "0" have no effect on the corresponding bit in the Power Down Control Register.

CONFIG +338h Clear Control for Power Down Control 4 Register PDN_CON4_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											APC	AFC	BPI	BSI		
Type											WC	WC	WC	WC		

This register is used to clear bits in the Power Down Control Register 4. When writing to this register each data bit which is "1" will causes the corresponding bit in the Power Down Control Register to be cleared to "0". Data bits which are "0" have no effect on the corresponding bit in the Power Down Control Register.

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